DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE -621 212

ELECTRONICS AND COMMUNICATION ENGINEERING

EC6304/LINEAR INTEGRATED CIRCUITS

QUESTION BANK

UNIT 1(2 MARKS)

1. **What is an integrated circuit? APRIL/MAY 2010**

   An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and Passive components fabricated together on a single crystal of silicon. The active components are Transistors and diodes and passive components are resistors and capacitors.

2. **What is current mirror? APRIL/MAY 2010**

   A constant current source (current mirror) makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage

3. **What are two requirements to be met for a good current source? MAY/JUNE 2012**

   a. Superior insensitivity of circuit performance to power supply variations and temperature.
   b. More economical than resistors in terms of die area required providing bias currents of small value.
   c. When used as load element, the high incremental resistance of current source results in high voltage gains at low supply voltages.

4. **What are all the important characteristics of ideal op-amp? APRIL/MAY 2015**

   Ideal characteristics of OPAMP

   1. Open loop gain infinite
   2. Input impedance infinite
   3. Output impedance low
   4. Bandwidth infinite
   5. Zero offset, ie, Vo=0 when V1=V2=0

5. **Define CMRR of OP-AMP APRIL/MAY 2011**

   The relative sensitivity of an op-amp to a difference signal as compared to a common - mode signal is called the common -mode rejection ratio. It is expressed in decibels.

   CMRR= Ad/Ac

6. **Define slew rate APRIL/MAY 2014**

The slew rate is defined as the maximum rate of change of output Voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

7. **Mention the advantages of integrated circuits over discrete components**. **APRIL/MAY 2014**

*Miniaturisation and hence increased equipment density.

*Cost reduction due to batch processing.

*Increased system reliability due to the elimination of soldered joints.

*Improved functional performance.

*Matched devices.

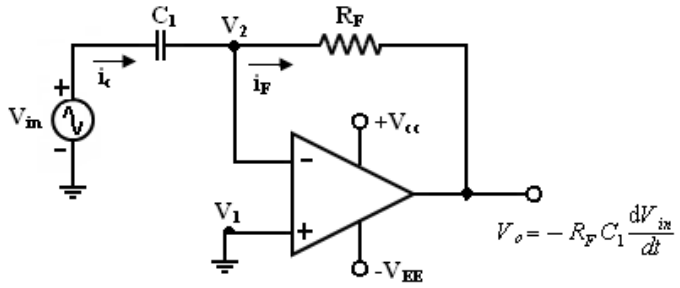
*Increased operating speeds.

*Reduction in power consumption.

8. **Define offset voltage of an Operational Amplifier**. **NOV/DEC 2013**

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

9. Draw the circuit diagram of differentiator and give its output equation. APRIL/MAY 2010



10. **List the various methods of realizing high input resistance in a differential amplifier. MAY/ JUNE 2012**

(i) Use of Darlington pair, (ii) Use of FET, (iii) Use of swamping resistance

UNIT-1 (16 MARKS)

1. **What is current Mirror? Discuss in detail a Widlar current source (16) APRIL/MAY 2008 ,NOV/DEC 2011(8), NOV/DEC2016(6)**

Constant current source (Current Mirror): (4)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage

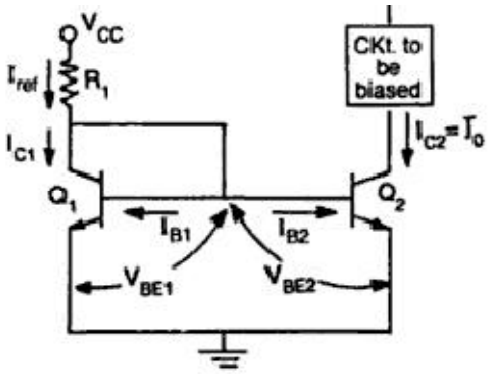


FIG:1 Current mirror circuit

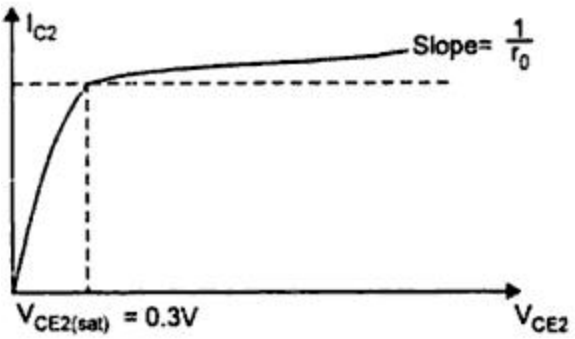
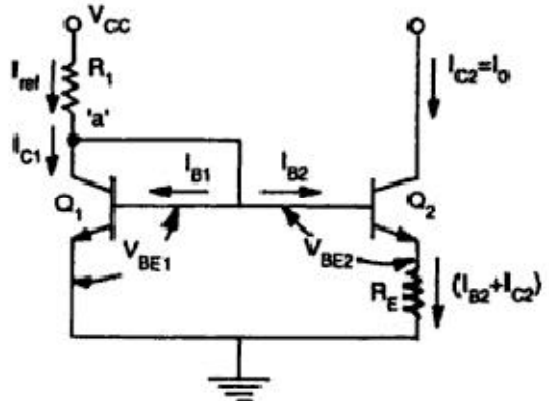


FIG:2 Current source output current characteristics

Widlar current source: (12)



Widlar current source which is particularly suitable for low value of currents

Iref= IC1+IB1+IB2
Iref = IC1 + IC1/β + IC2/β
NeglectingIC2/β, Iref = IC1(1 +)
Iref = V_{CC}-V_{BE}/R_1
When β>> 1, IC1 = Iref

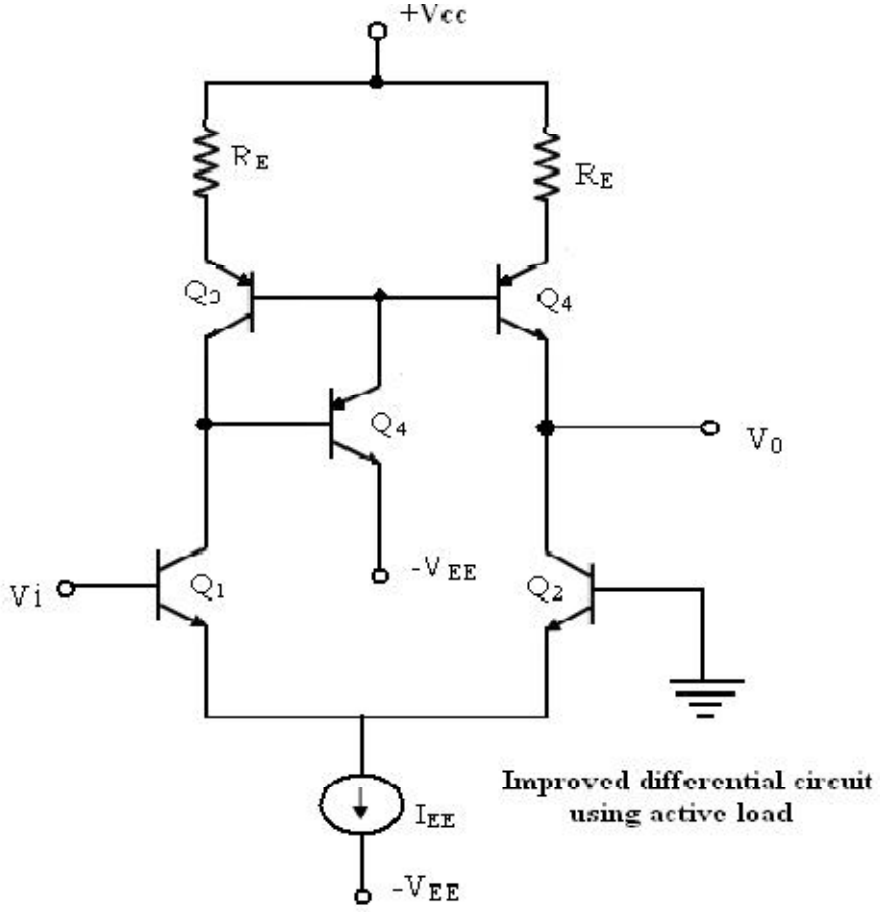
2. **(i) Define CMRR. Draw the circuit of an Op-amp differential amplifier and give theexpression for CMRR. (8) APRIL/MAY 2010**

CMRR (2)

The relative sensitivity of an op-amp to a difference signal as compared to a common - mode signal is called the common -mode rejection ratio. It is expressed in decibels.

CMRR= Ad/Ac

Circuit of an Op-amp differential amplifier (6)



Improved differential circuit using active load

CMRR=20 log $_{10}|A_{dm}/A_{cm}|$dB

Balanced case

CMRR=20 $\log_{10}$ $|R_S+h_{Ie}+2R_E(1+h_{fe})/(R_S+h_{ie})|$Db

UnBalanced case

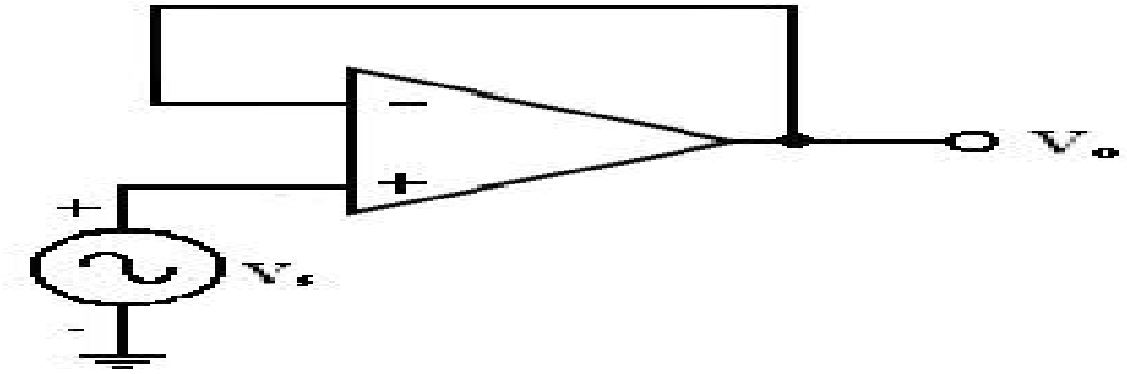
CMRR=20 $\log_{10}$ $|R_S+h_{Ie}+2R_E(1+h_{fe})/2(R_S+h_{ie})|$dB

(ii) Define Slew Rate. Explain the cause of slew rate and derive an expression for Slew rate for an op-amp voltage follower. (8) APRIL/MAY 2010 , APR/MAY2017(8)

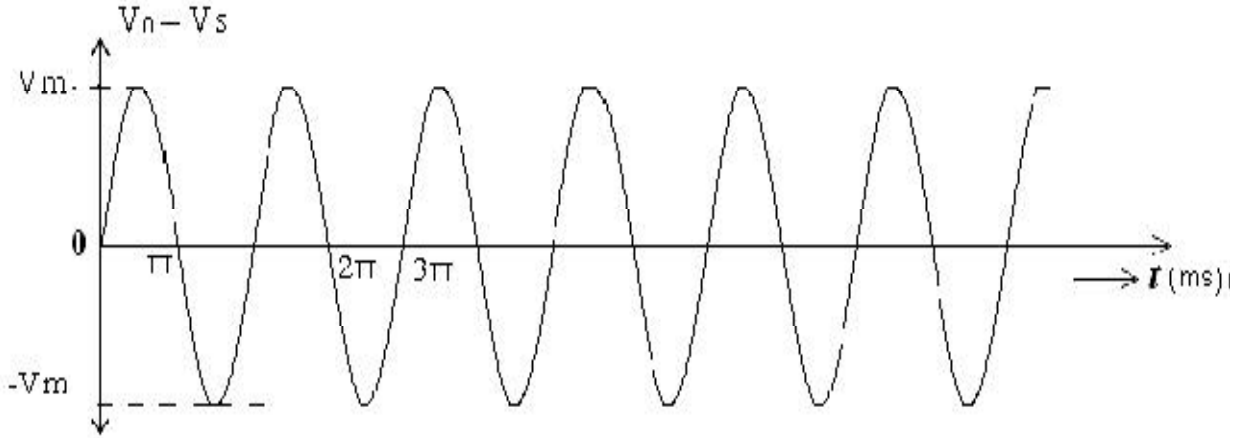
Slew Rate (2)

Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs.

Reason for Slew rate: (6)



Voltage Follower Circuit



Input and output waveforms of a voltage follower

The max rate of change of output across when coswt =1

(i.e) SR =dV0/dt |max = wVm.

SR = 2 fVm V/s = 2 fVm v/ms.

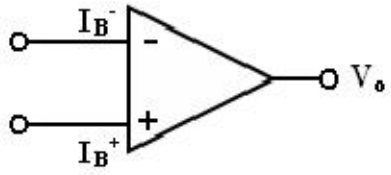
Thus the maximum frequency fmax at which undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

3. **(i)List and Explain the non-ideal DC characteristics of an operational amplifier (8) MAY/JUNE 2012, APR/MAY2017(8)**

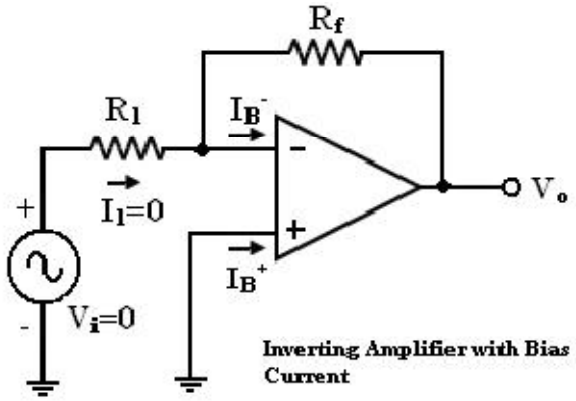
Non-ideal DC characteristics:

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

Input bias current:



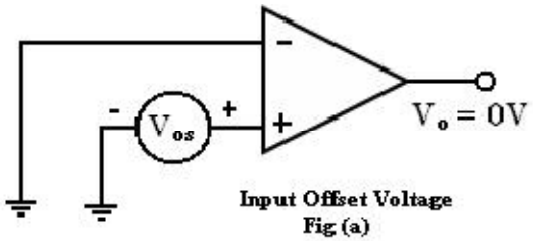
Input Bias Current



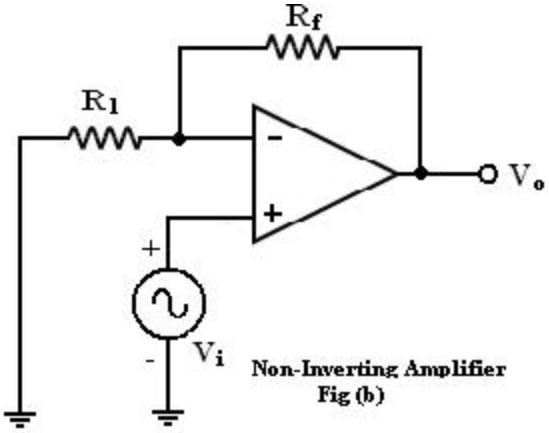
Inverting Amplifier with Bias Current

Input offset current:

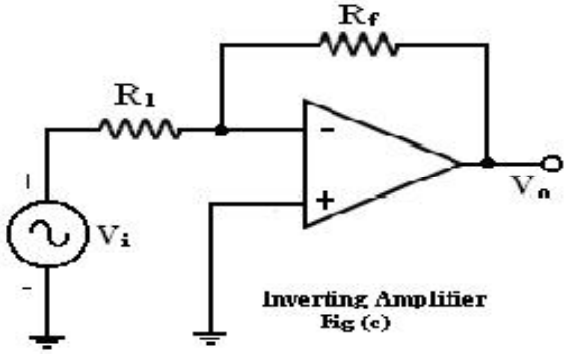
Input offset voltage:



Input Offset Voltage
Fig (a)



Non-Inverting Amplifier
Fig (b)



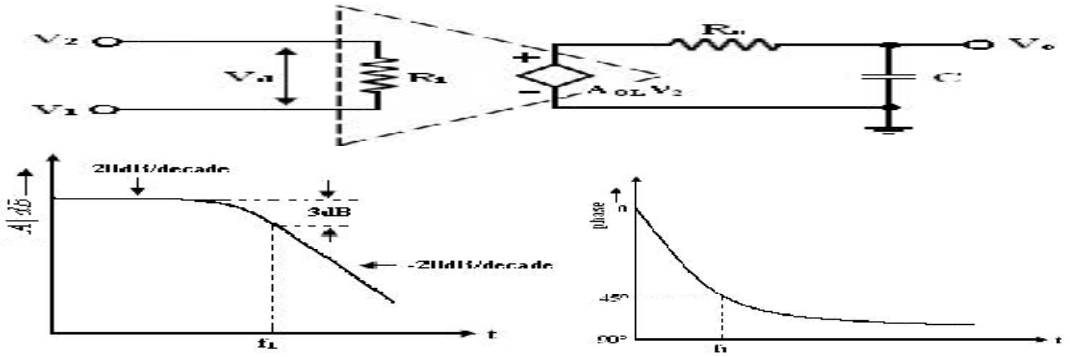
Inverting Amplifier
Fig (c)

Thermal drift

(ii)Explain the ideal AC characteristics of an operational amplifier (8)
MAY/JUNE 2012 , APR/MAY 2017(16)

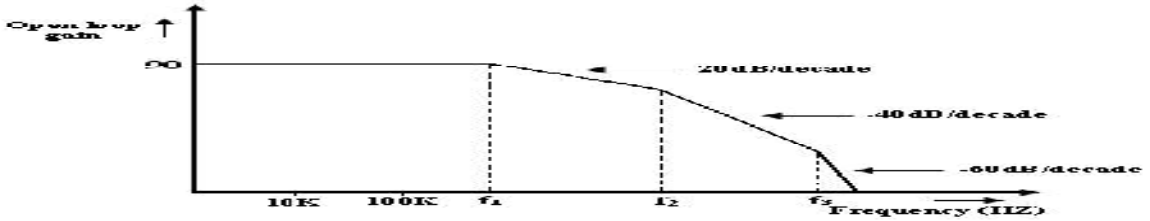
Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response

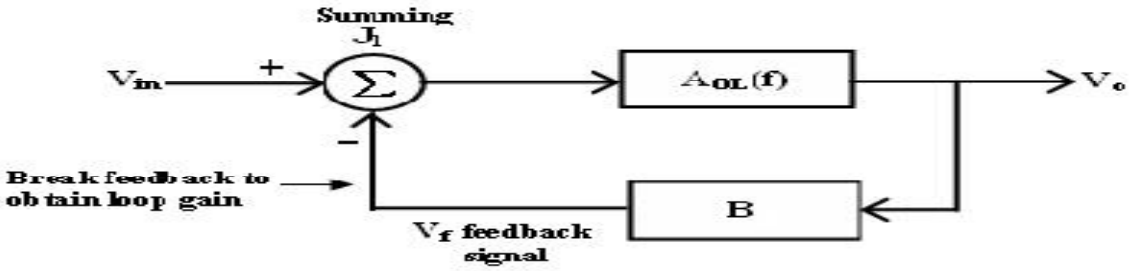


Frequency response of op amp

Roll off rate of op amp gain



Circuit Stability:



Feedback loop system

The closed loop gain Af is given by AF = V0 /Vin
= AOL / (1+(AOL) (B) ----(2)
B = gain of feedback circuit.

1. Method 1:

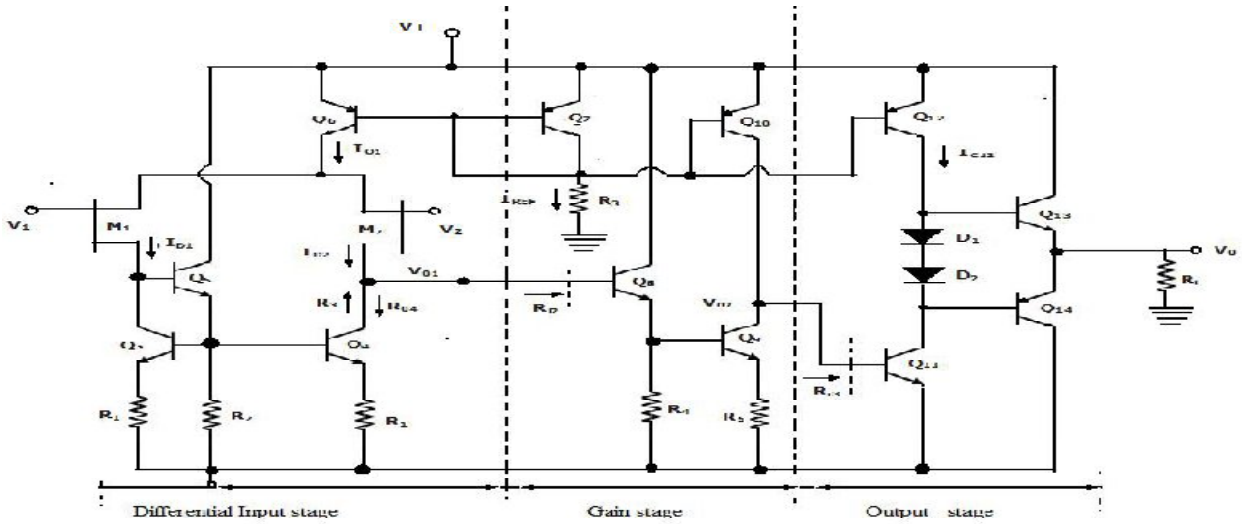
Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.
If phase angle is >-180 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.

If phase angle is > - 180 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

4. **Explain the Integral circuit diagram of IC741.Discuss its AC and DC performance characteristics NOV/DEC 2010 , MAY/JUNE 2014 ,NOV/DEC2015(16)**
   Integral circuit diagram of IC741 (8)



An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

IC 741 Bipolar operational amplifier (8)

AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as

Frequency response

The variation in operating frequency will cause variations in gain magnitude and its phase angle.

The manner in which the gain of the op-amp responds to different frequencies is called the Frequency response

slew-rate.

Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs.

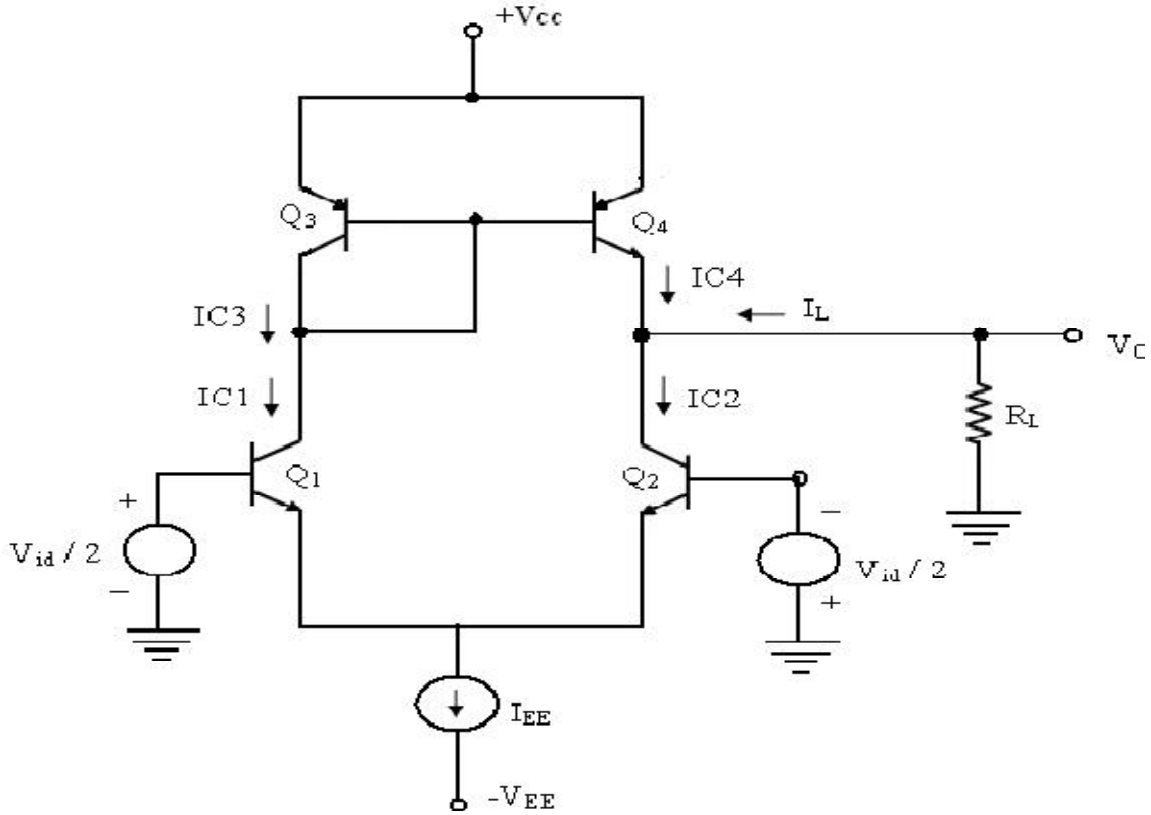
DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

5. Draw the circuit of a differential amplifier with current Mirror load. Draw its equivalent circuit and derive an expression for its gain MAY/JUNE 2007



IC4 = IC3 = IC1 = gmVid/2 where IC4 = IC3 due to current mirror action.

IC2 = - gmVid/2 .

We know that the load current IL entering the next stage is

IL= IC2-IC4 = - gmVid/2 - gmVid/2 = - gmVid

Analysis of BJT differential amplifier with active load:

The collector currents of all the transistors are equal.

IC1 = IC2 = IC3 =IC4 = IEE/2 .

The Collector -emitter voltages of Q1 and Q2 are given by

VCE1-VCE2 =VC-VE=V CC - VEB-(-VEB)= VCC

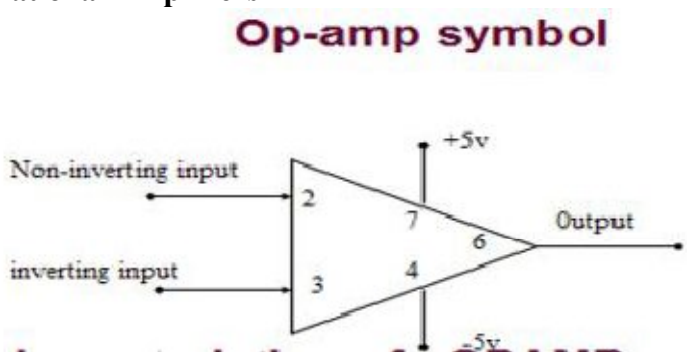
Eqn. shows that, the offset is higher than that of a resistive loaded differential amplifier A. This can be reduced by the use of emitter resistors for Q 3 and Q 4 , and a transistor Q5 in the current mirror load

6. (i) With neat Block Diagram ,explain the general stages of an OP-AMP IC
Basic information about operational amplifiers NOV/DEC 2011 (8)

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.

It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

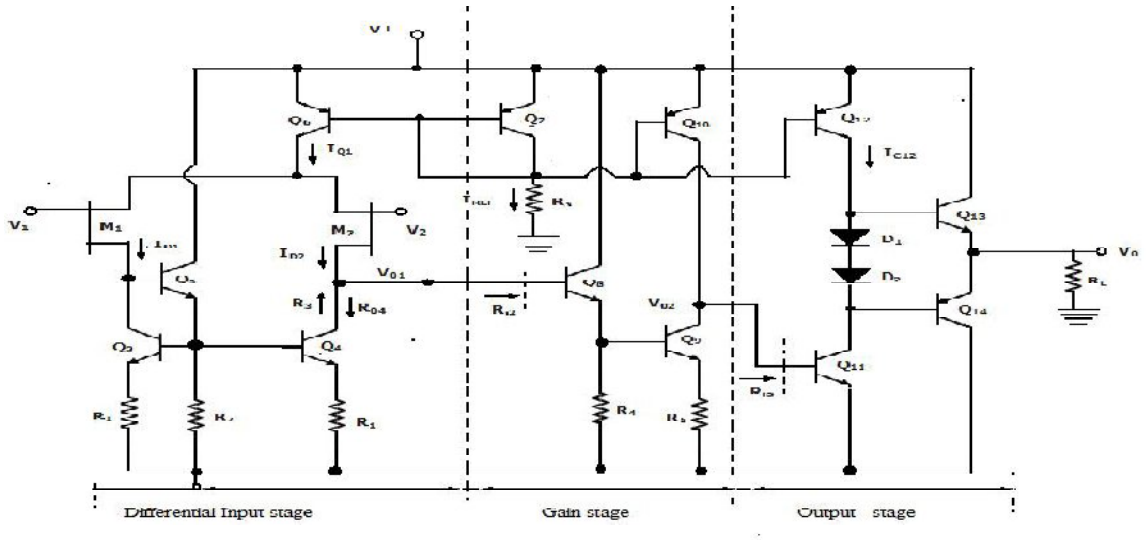
Ideal operational Amplifiers



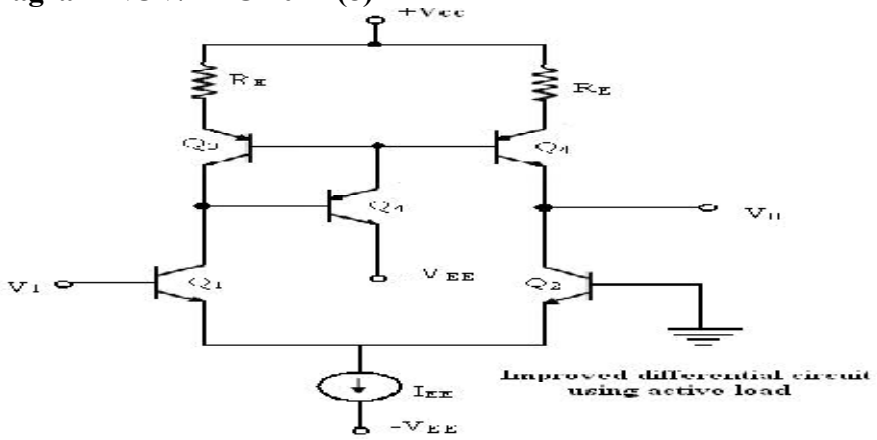
General Operational Amplifier stages and internal circuit diagrams of IC 741

An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.



(ii)Explain the circuit diagram , the working of BJT Emitter coupled differential amplifier. Also explain the concept of active load and sketch the relevant circuit Diagram NOV/DEC 2011 (8)



Improved differential circuit using active load

BJT Differential Amplifier using active loads:

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q3 and Q4 with the transistor Q3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by

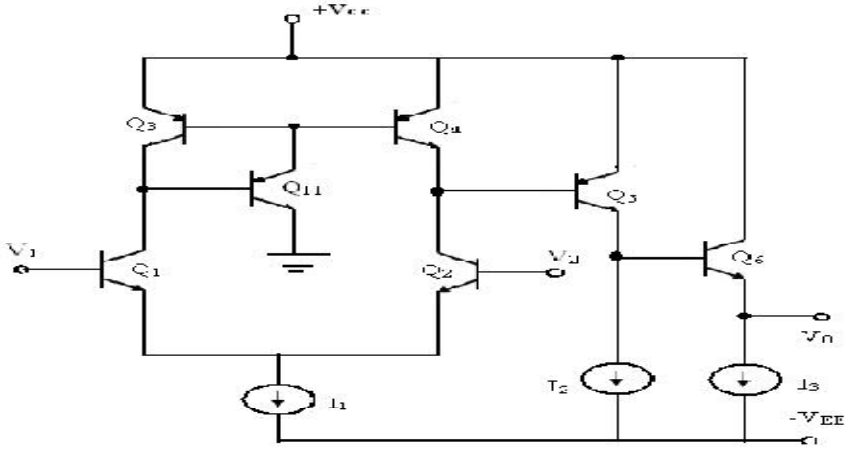
IC4 = IC3 = IC1 = gmVid/2

Where IC4 = IC3 due to current mirror action.

IC2 = - gmVid/2 .

We know that the load current IL entering the next stage is

IL= IC2-IC4 = - gmVid/2 - gmVid/2 = - gmVid



BJT Differential Amplifier with additional output stage

Analysis of BJT differential amplifier with active load:

The collector currents of all the transistors are equal.

IC1 = IC2 = IC3 =IC4 = IEE/2 .

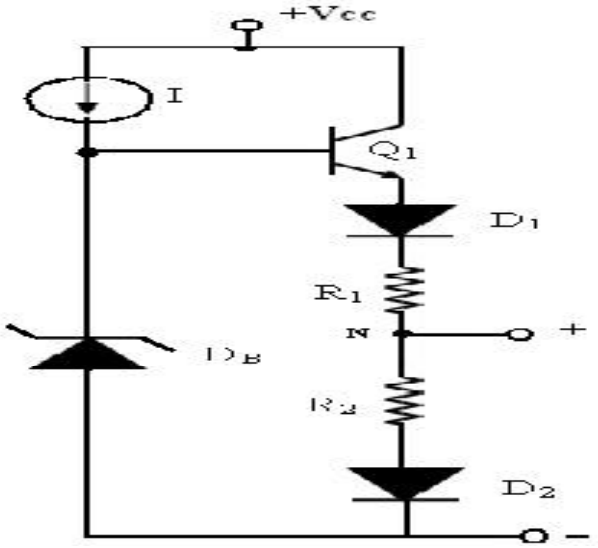
The Collector -emitter voltages of Q1 and Q2 are given by

VCE1-VCE2 =VC-VE=V CC - VEB-(-VEB) = VCC

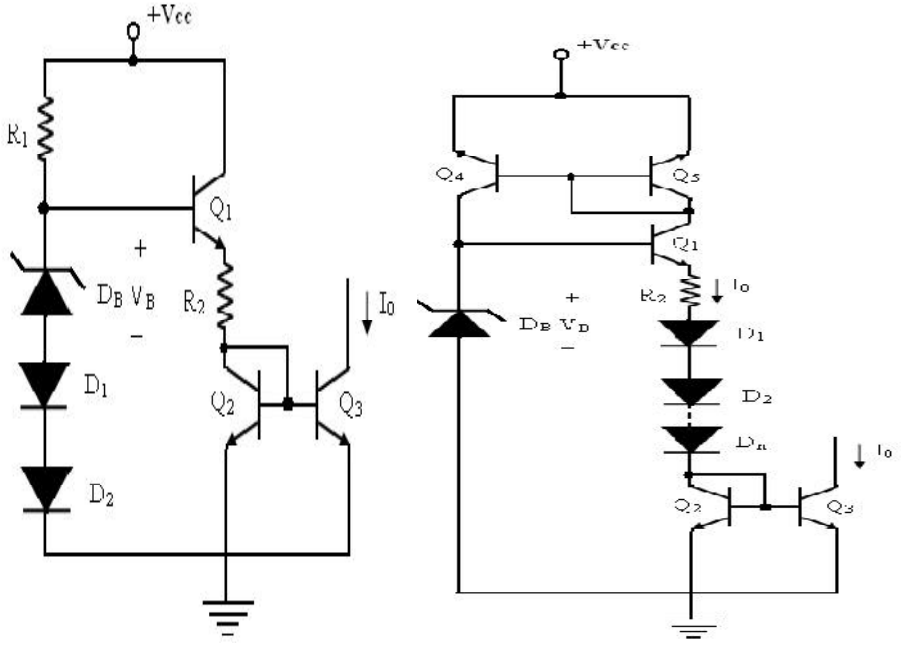
7. **(i) With neat circuit Diagrams , explain the operations of (i) voltage reference circuit using temperature compensation (ii) voltage reference circuit using avalanche diode reference (12) MAY/JUNE 2012**

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output reference voltage TCR

Voltage Reference circuit using temperature compensation scheme(6)



Voltage Reference circuit using Avalanche Diode Reference: (6)



(ii) Current Mirror problem (4)

UNIT 2 (2 MARKS)

1. **What is a VCO? APRIL/MAY 2010**

Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the free running frequency. This frequency can be shifted to either side by applying a dc control voltage and the frequency deviation is proportional to the dc control voltage.

2. **What is comparator? MAY/ JUNE 2012**

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is an open loop op - amp with output + Vsat .

3. **Why active guard drive is necessary for an instrumentation amplifier? MAY/ JUNE 2012**

(i) Due to ground loop interference additional voltage drop gets inserted which may cause error in low level measurements.

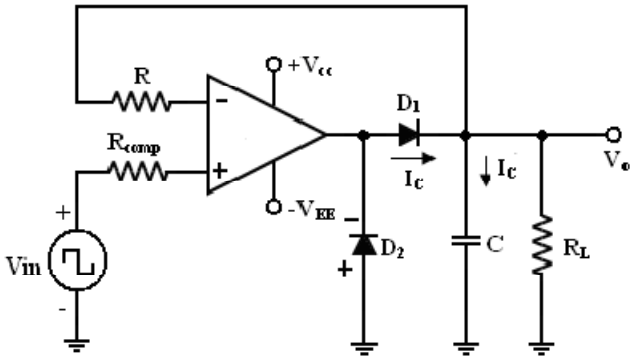
(ii) Due to distributed cable capacitances there is degradation of CMRR.

The active guard drive eliminates all these problems and necessary for an instrumentation amplifier.

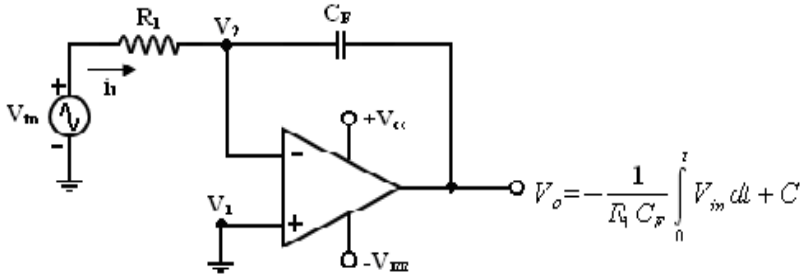
4. **What is a voltage follower? APRIL/MAY 2014**

A circuit in which output follows the input is called voltage follower.

5. **Draw the circuit diagram of peak detector. APRIL/MAY 2014**



6. **Draw and write equation of an integrator using an op-amp. NOV/DEC 2010**



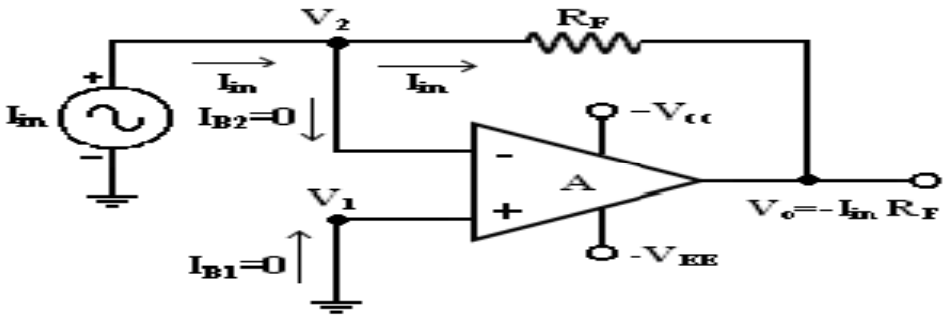
7. **Why active guard drive is necessary for an instrumentation amplifier? MAY/ JUNE 2012**

(i) Due to ground loop interference additional voltage drop gets inserted which may cause error in low level measurements.

(ii) Due to distributed cable capacitances there is degradation of CMRR.

The active guard drive eliminates all these problems and necessary for an instrumentation amplifier.

8. **Give the schematic of op-amp based current to voltage converter. APRIL/MAY 2010**



At node V_2, $V_1=V_2=0$

$I_{in} = -V_0 / R$

$V_0 = - I_{in} R$, $V_0 \propto I_{in}$

9. **Compare the performance of inverting and non inverting operational amplifier configurations. NOV/DEC 2010**

Inverting amplifier	Non inverting Amplifier
1. Gain = -Rf / R1 2. Input impedance is R1 3. Gain adjusted as greater than, less than or equal to one. 4. Output is inverted w.r.to input	1. Gain = 1+(Rf/R1) 2. Input impedance very large 3. Gain is always greater than one. 4. No phase shift between input and output.

10. **What are the applications of comparator? APRIL/MAY 2008**

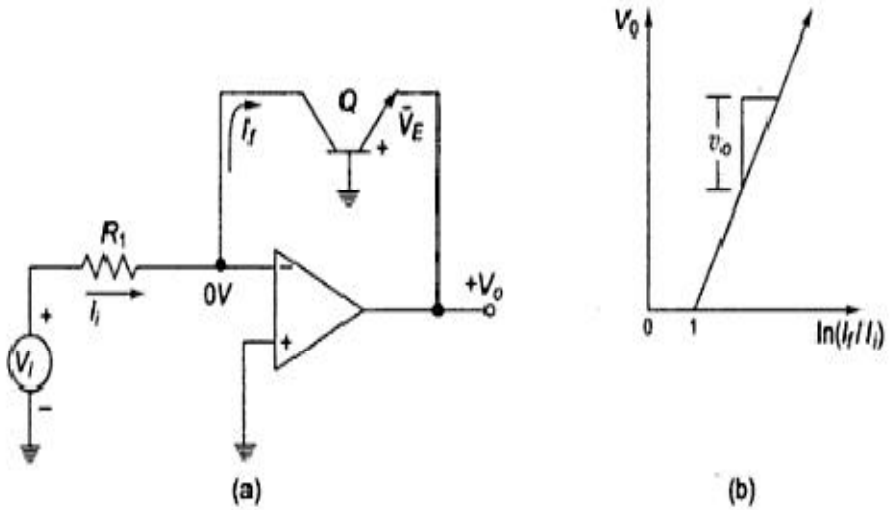
1.Zero crossing detector
2.Window detector
3.Time marker generator
4.Phase detector

UNIV 2 (16 MARKS)

1. **(i) construct a logarithmic amplifier with OP-AMP and derive the Expression for the output voltage (8)APRIL/MAY 2015 , APRIL/MAY 2008**

Log Amplifier:

$$V_o = V_i ln\left(I_f / I_i\right)$$

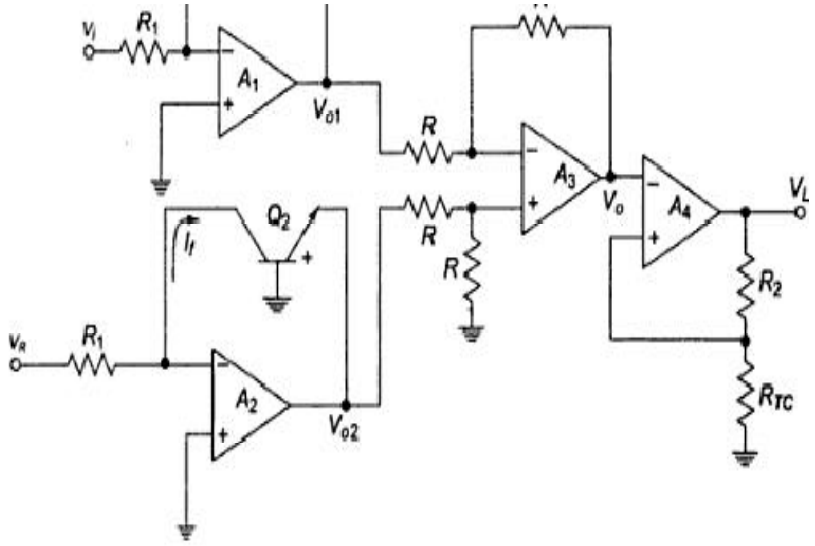


Uses:

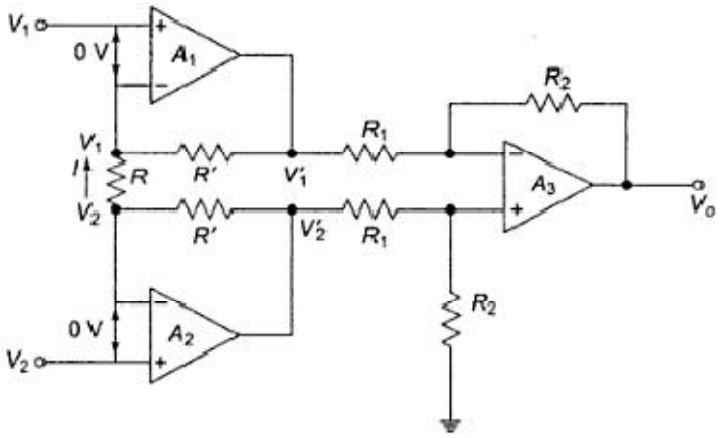
Direct dB display on a digital Voltmeter and Spectrum analyzer.
Log-amp can also be used to compress the dynamic range of a signal.

$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

Logarithmic amplifier with compensation of emitter saturation current



(ii) **Explain the Instrumentation Amplifier circuit and obtain Expression for gain .What are its applications (8) NOV/DEC 2013 MAY/JUNE 2013**



Current flowing in resistor R is I= (V1-V2)/R and it flow through R' in the direction shown, Voltage at non-inverting terminal op-amp A3 is R2V1'/(R1+R2). By superposition theorem,

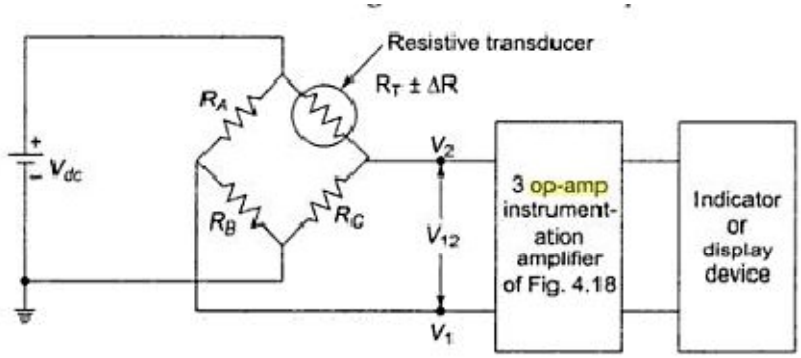
Vo= (R2/R1)V1+(1+R2/R1)(R2V2/(R1+R2)=R2/R1(V1'-V2');

V1'= R'I+V1=R'/R(V1-V2)+V1

V2'= R'I+V1=R'/R(V1-V2)+V2;V0= (R2/R1)[(2R'/R(V2-V1)+ (V2-V1)]= (R2/R1)[(1+2R'/R)(V2-V1)

Important features of an instrumentation amplifier are

1. High gain accuracy
2. High CMRR
3. High gain stability with low temperature coefficient
4. Low output impedance

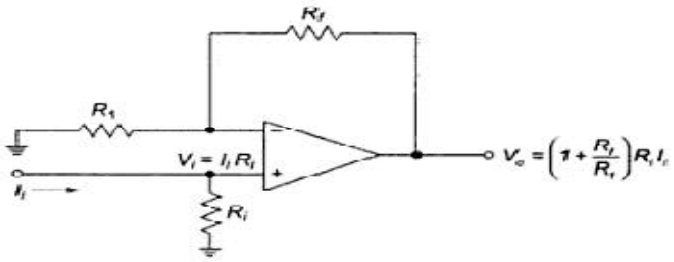


Applications of instrumentation amplifier with the transducer bridge,

- o temperature indicator,
- o temperature controller and
- o light intensity meter .

2. Discuss the following applications of OP-AMP APRIL/MAY 2015

(i) Current to voltage Converter(8)

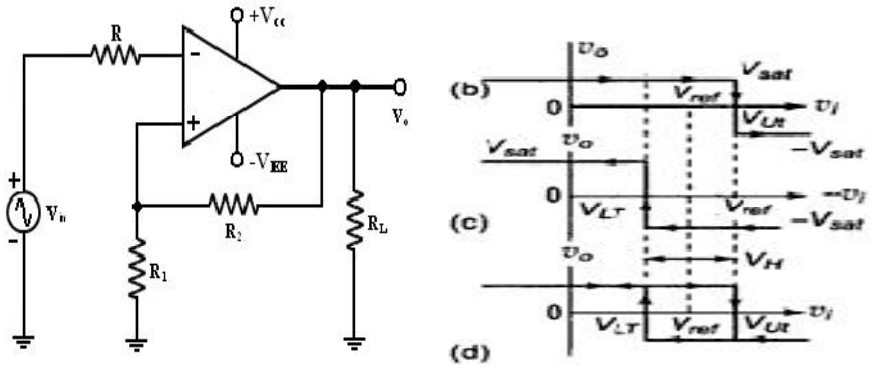


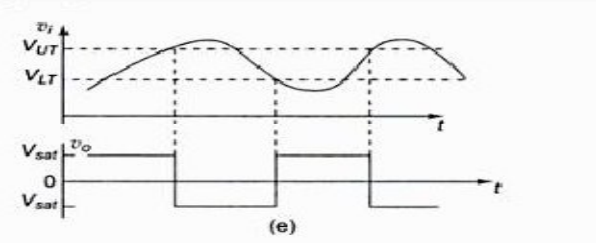
Sensitivity of the I – V converter:

1. The output voltage V0 = -RF Iin.
2. Hence the gain of this converter is equal to -RF. The magnitude of the gain (i.e.) is called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV0 for a given change in the input current ΔIin is decide by the sensitivity of I-V converter.
4. By keeping RF variable, it is possible to vary the sensitivity as per the requirements.

(ii) **Schmitt Trigger: [Square Circuit] (8) APRIL/MAY 2015 , APRIL/MAY 2008 (16) MAY/JUNE 2012 (8) NOV/DEC2013 (8)**

This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V0 every time it exceeds certain voltage levels called the upper threshold and lower threshold voltage.



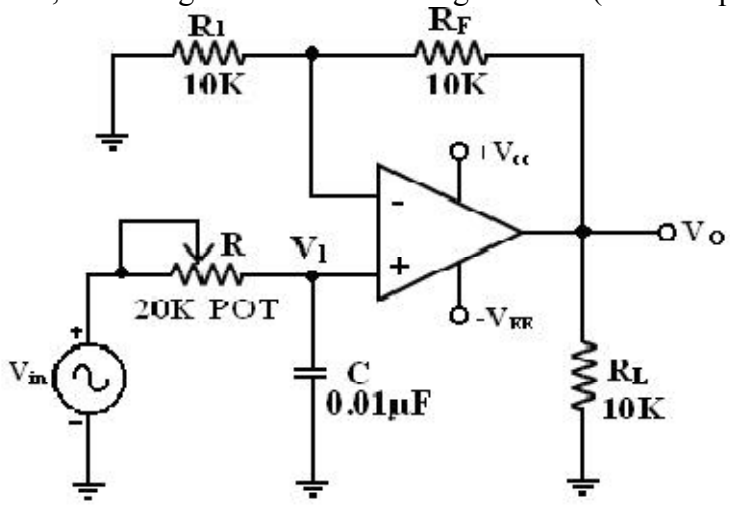


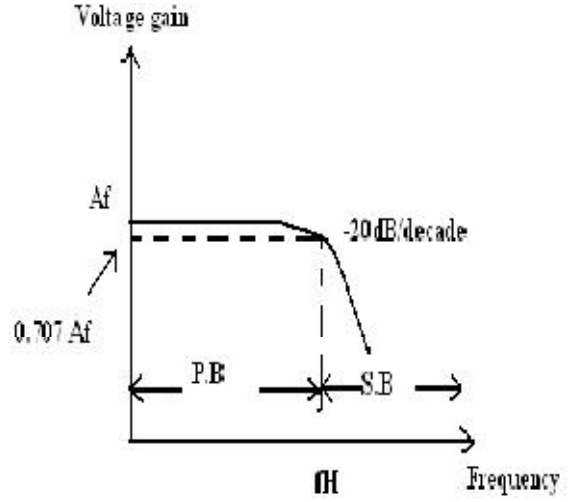
Schmitt Trigger as squarer

3. (i) Design a First order LPF filter(8) APRIL/MAY 2010

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & Rf determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,





1. At very low frequency, f < fH

$|H(j\omega)| = A$

2. At f =fH

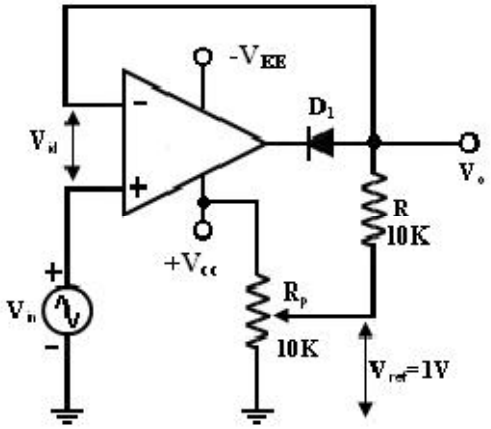
$|H(j\omega)| = A/\sqrt{2} = 0.707A$

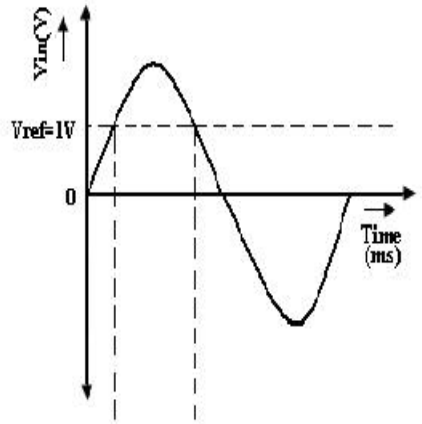
3. At f> fH

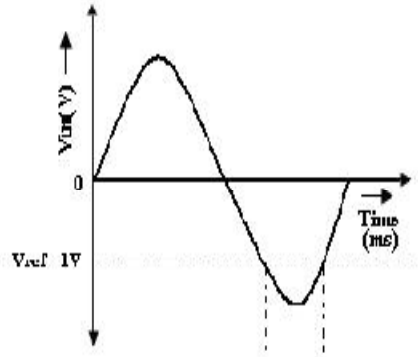
$|H(j\omega)| << A \cong 0$

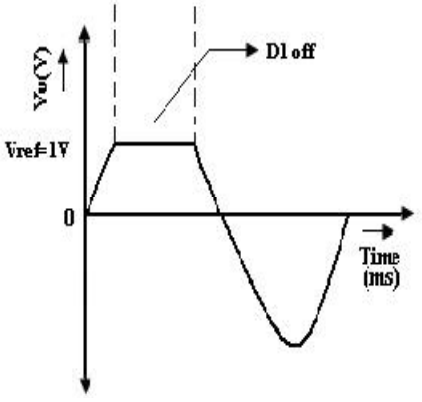
(ii) Explain the positive clipper circuit using an OP-AMP and a diode with neat diagram(8)
APRIL/MAY 2010

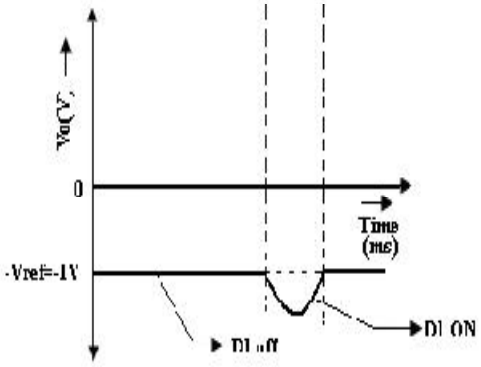
A circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. T he clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp (Vref < Vin). The Output voltage has the portions of the positive half cycles above Vref clipped off.









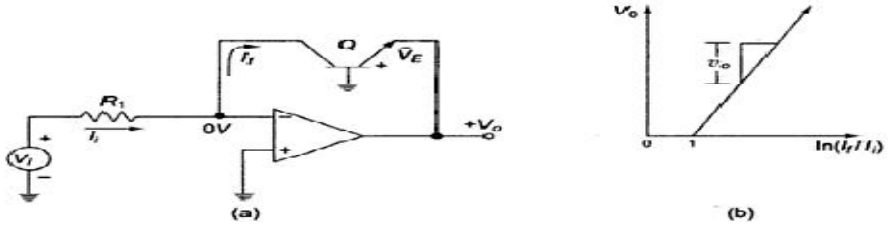


4. **With neat diagram explain logarithmic amplifier and anti logarithmic amplifier APRIL/MAY 2014**

Logarithmic Amplifier

Antilog computation may require functions such as ln x, log x or sin hx.

$$V_o = V_i ln\ (I_f / I_i)$$



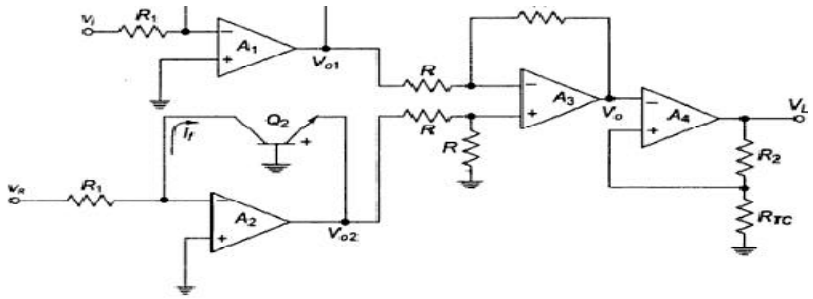
Uses:

Direct dB display on a digital Voltmeter and Spectrum analyzer.

Log-amp can also be used to compress the dynamic range of a signal

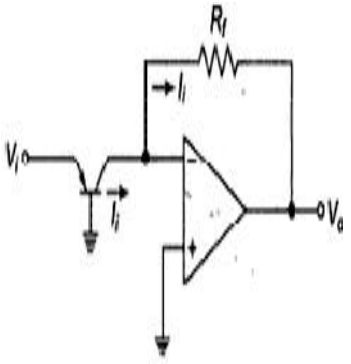
$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

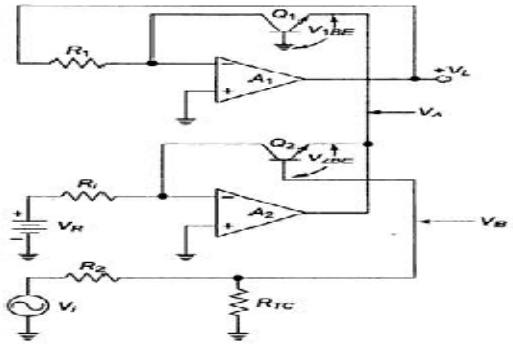
Logarithmic amplifier with compensation of emitter saturation current



Antilog Amplifier

A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents

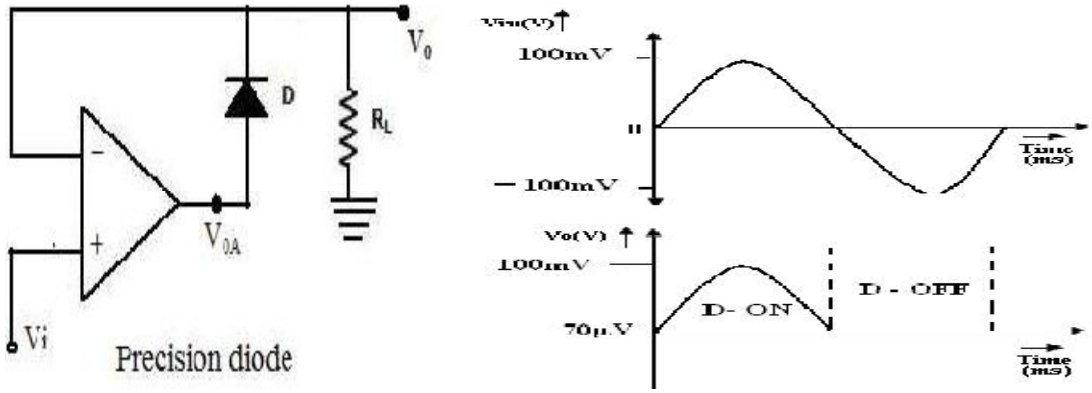




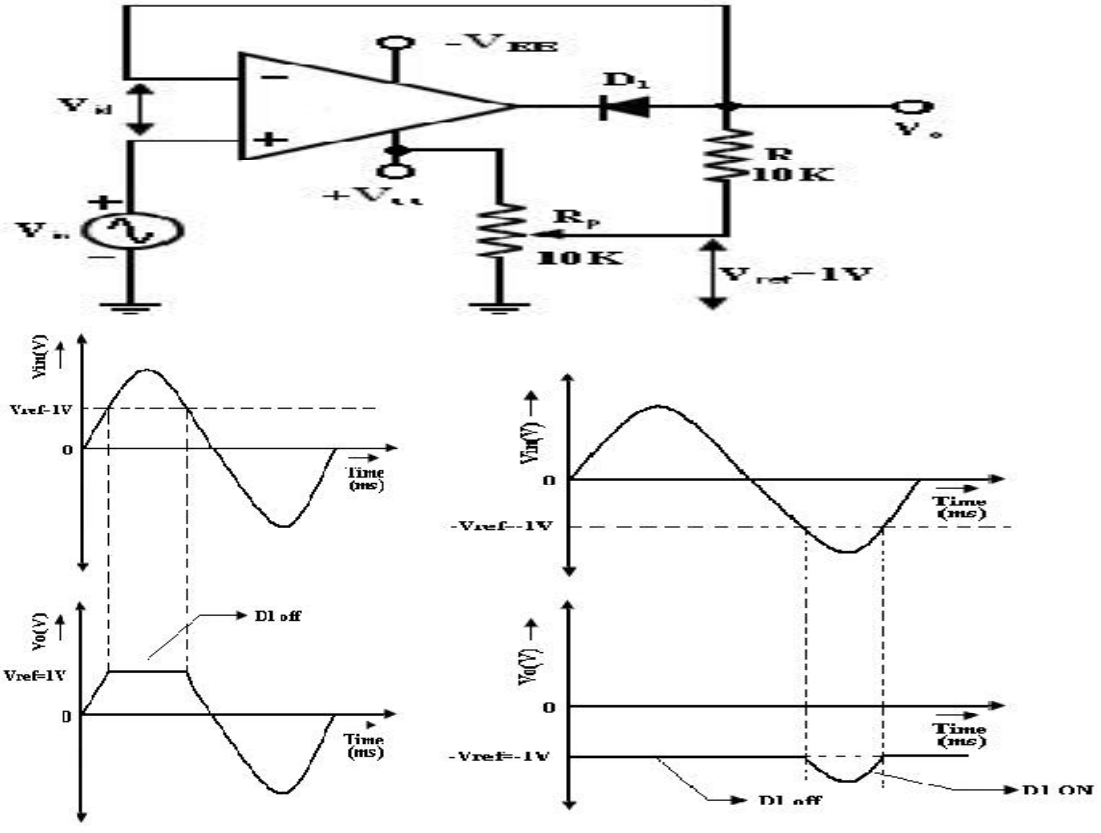
5. With neat diagram explain the application of OP-AMP as precision Rectifier, clipper, clamper APRIL/MAY 2014

Precision Rectifier: (6)

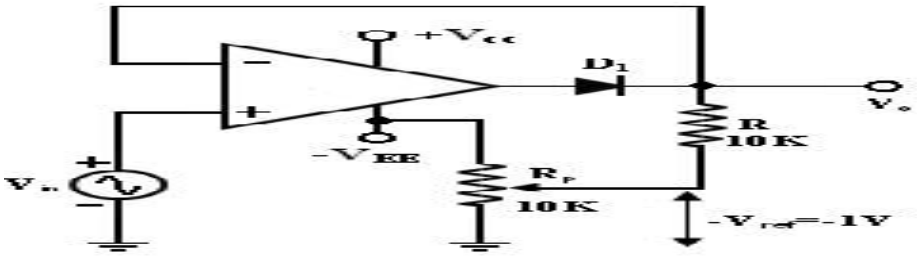
The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

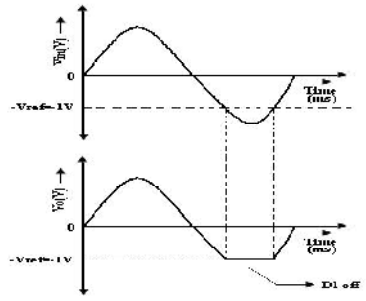


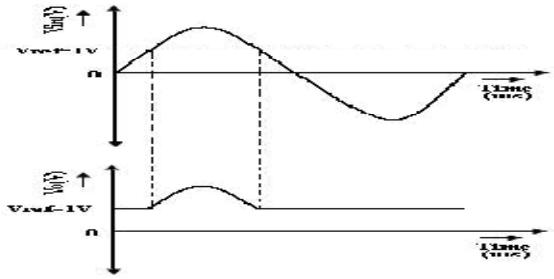
Clipper: Positive Clipper: (5)



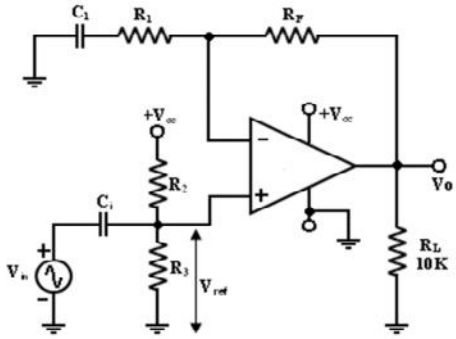
Negative Clipper:

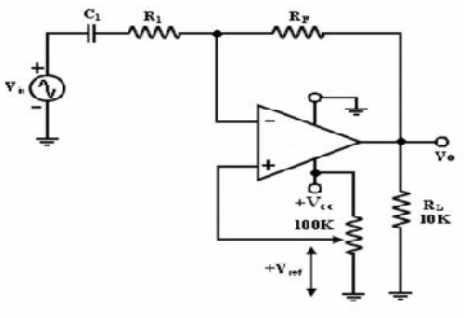


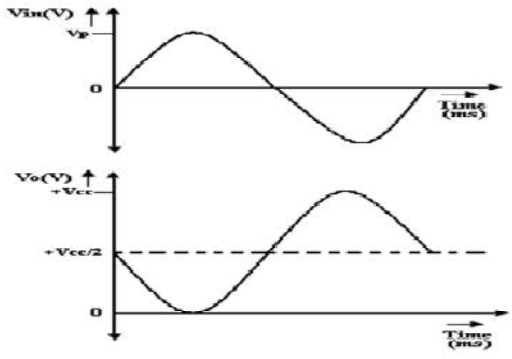


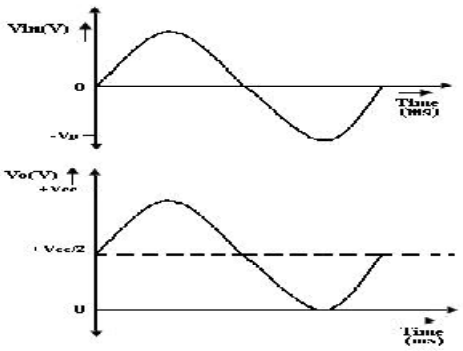


Positive and Negative Clampers: (5)



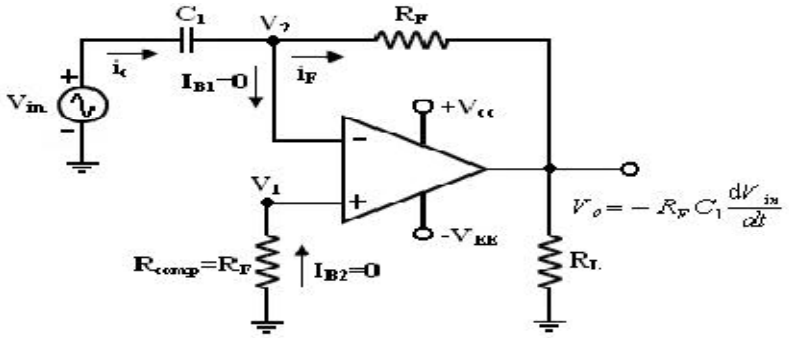


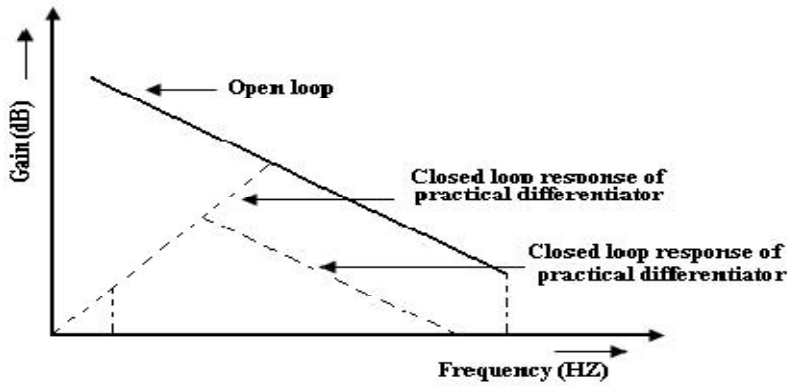




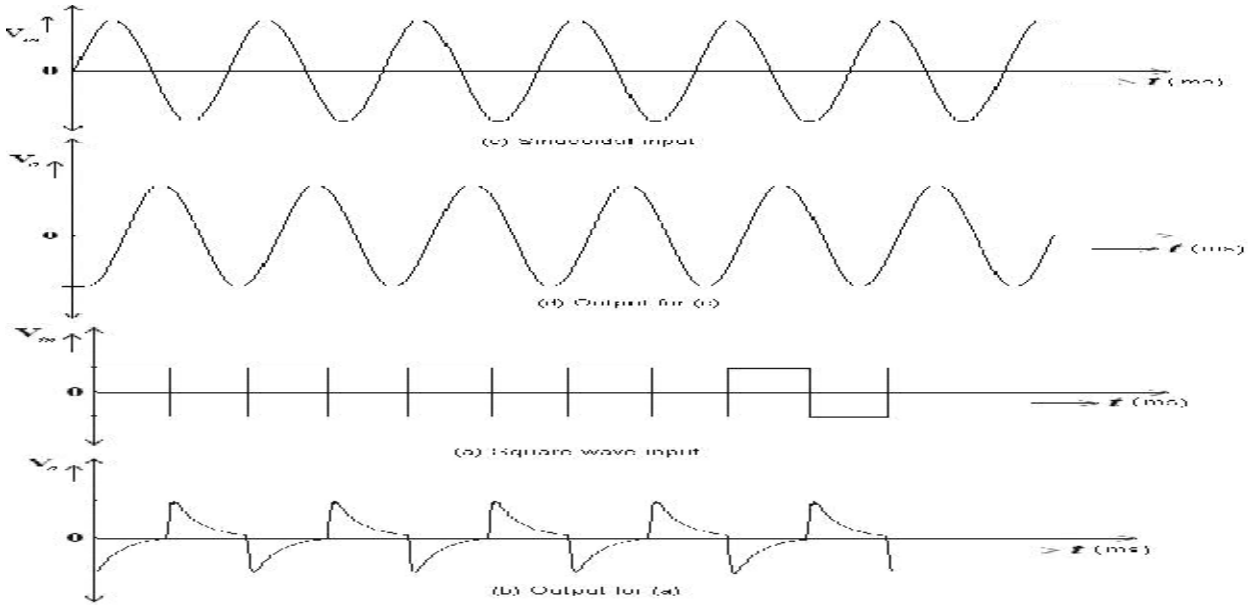
6. (i)Sketch the basic circuit using op-amp to perform the mathematical operation of differentiation and explain. What are the limitations of an ordinary OP-AMP differentiator? MAY/JUNE 2012

The circuit performs the mathematical operation of differentiation (i.e.) the output waveform is the derivative of the input waveform



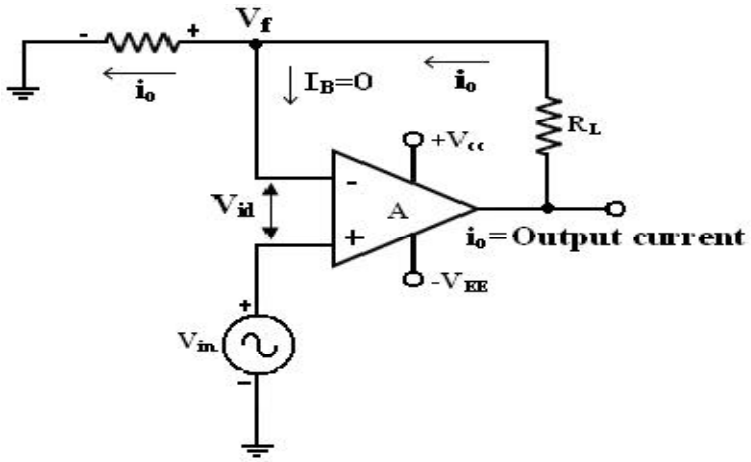


Frequency response of differentiator



(ii) **Draw and Explain the circuit of voltage to current converter if the load is (i) Floating (ii) Grounded MAY/JUNE 2012**

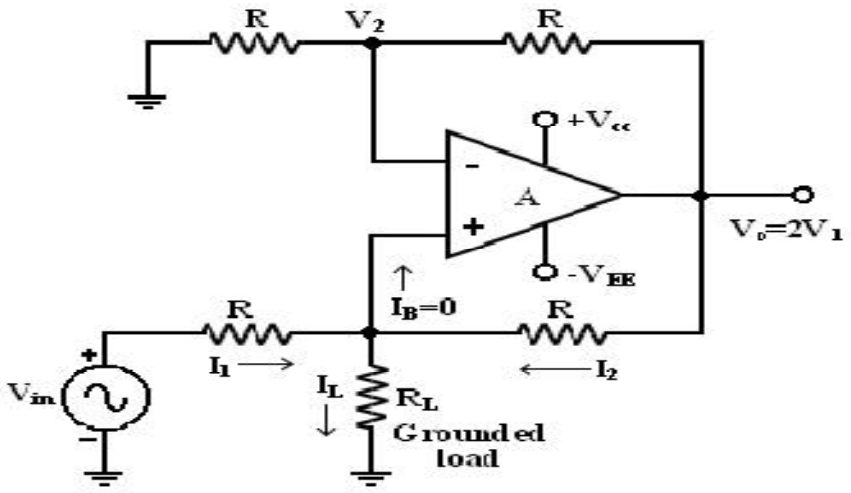
Voltage to Current Converter with floating loads (V/I):(4)



Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

Voltage – to current converter with Grounded load:(4)



Analysis of the circuit:

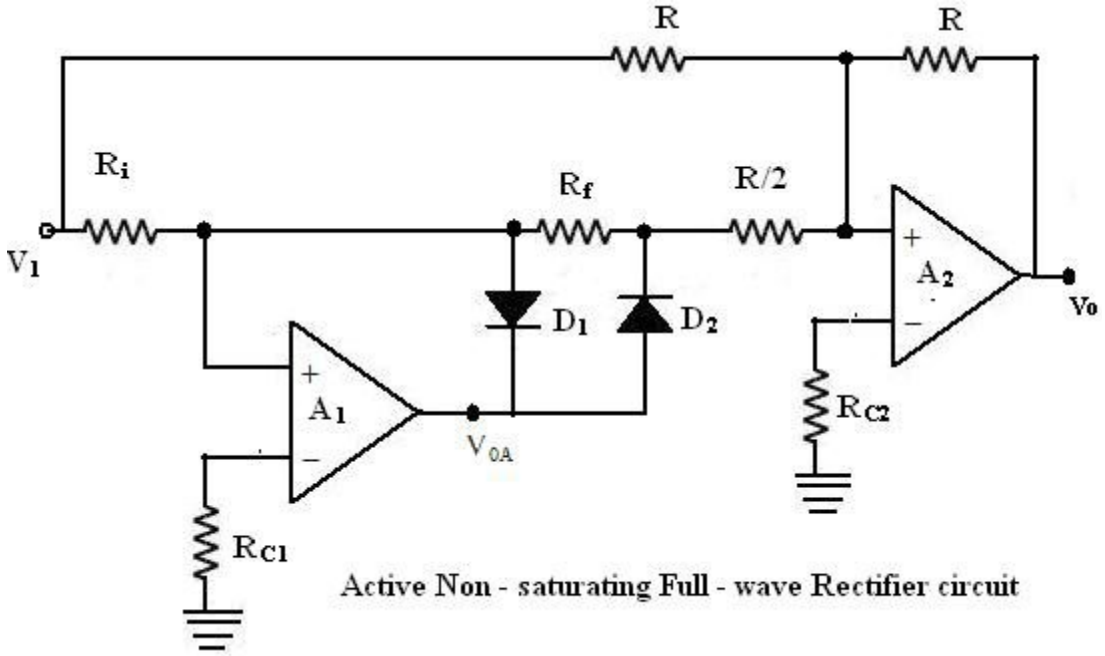
The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V1 at the non-inverting (+) terminals and
2. To establish relationship between V1 and the load current IL

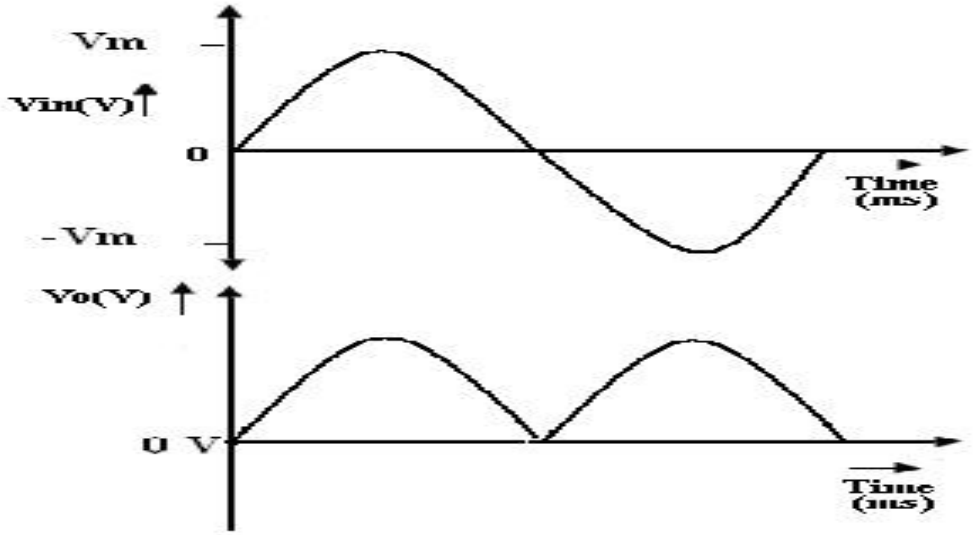
7. Explain the working of (i) precision full wave Rectifier (ii) integrator NOV/DEC 2013

(i) precision full wave Rectifier (8)

The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier.



Active Non - saturating Full - wave Rectifier circuit



Input and Output Waveforms

To summarize the operation of the circuit,

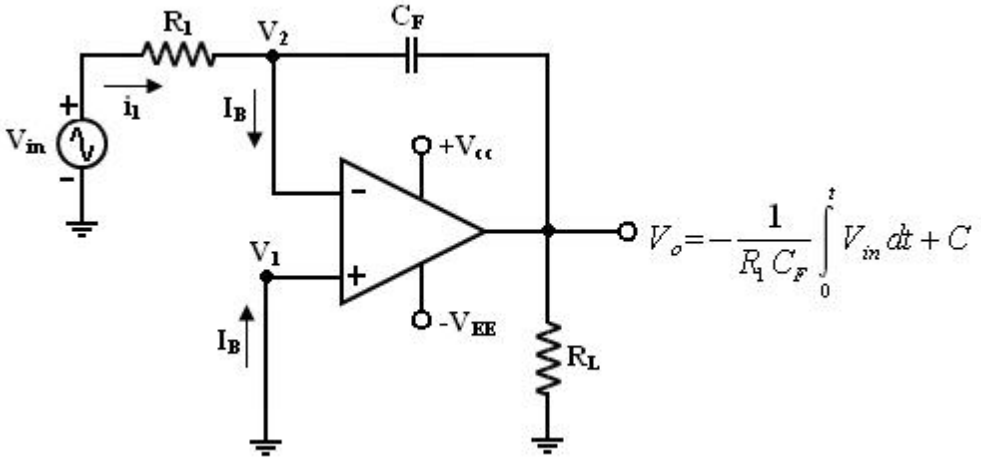
V0 = Vi when Vi < 0V and

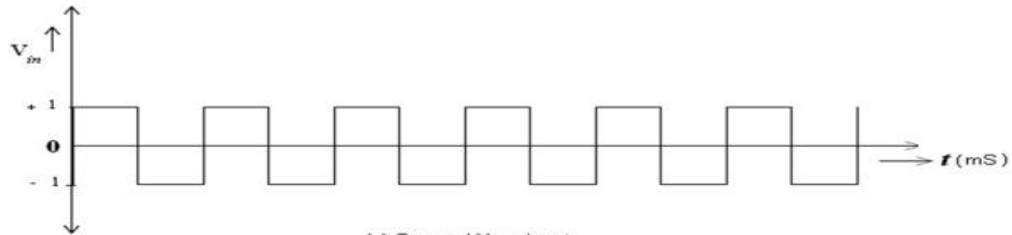
V0 = Vi for Vi > 0V, and hence

V0 = |Vi |

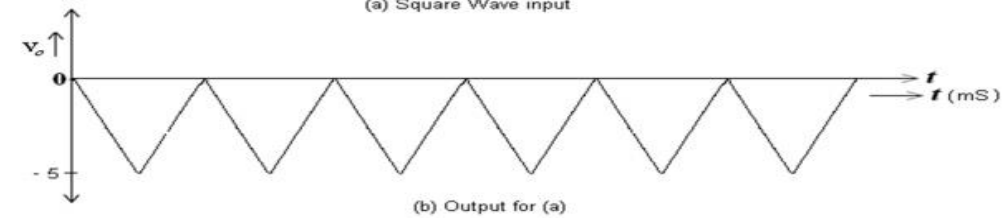
(ii)Integrator MAY/JUNE 2013

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier.

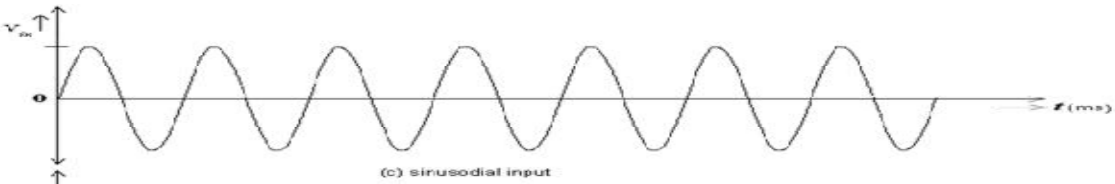




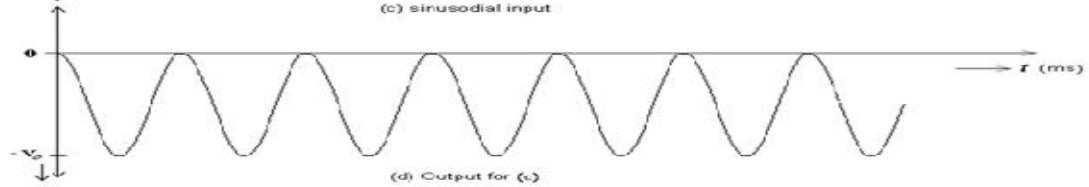
(a) Square Wave input



(b) Output for (a)



(c) sinusodial input



(d) Output for (c)

UNIT 3 (2 MAKS)

1. **Define resolution of a data converter. APRIL/MAY 2010**

   The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

   Resolution (in volts)= $V_{OFS}/2^n$-1

   The resolution of an ADC is defined as the smallest change in analog input for a one bit change at the output.

2. **What is lock range and capture range of PLL? NOV/DEC 2010**

   Lock range

   The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.

   Capture range

   The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.

3. **What are the advantages of variable transconductance technique? MAY/ JUNE 2012**

   (i) Simple to integrate into monolithic IC

   (ii) Provide very good accuracy, four quadrant operation.

   (iii) Reduce error at least by 10 times.

4. **VCO is also called as V-f converter. Why? MAY/ JUNE 2012**

   Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the free running frequency. This frequency can be shifted to either side by applying a dc control voltage and the frequency deviation is proportional to the dc control voltage.

   Input voltage is converted into output frequency so it is also called V-f converter.

5. **Define capture range of PLL. NOV/DEC 2011**

   The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is expressed as a percentage of the VCO free running frequency.

6.

7. **What is meant by frequency synthesizing NOV/DEC 2013**

   A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc. A frequency synthesizer can combine frequency multiplication, frequency division, and frequency mixing (the frequency mixing process generates sum and difference frequencies) operations to produce the desired output signal.

8. **Define lock range of PLL NOV/DEC 2013**

   The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. It is expressed as a percentage of the VCO free running frequency.

9. What is FSK technique APRIL/MAY 2008

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

10. Mention any two applications of PLL MAY/ JUNE 2013

- Frequency multiplication/division
- Frequency translation c. AM detection
- FM demodulation
- FSK demodulation.

UNIT III (16 MARKS)

16 MARKS

1. **Explain the applications of Phase Locked Loop (16) NOV/DEC 2015, MAY/JUNE2012 (16) , MAY/JUNE2014(16),APR/MAY2017 (7), MAY/JUNE2013(8), NOV/DEC2013 (6)**

(i)Frequency synthesizer (ii) AM demodulator (iii) FM Demodulator

Frequency synthesizer

A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including

radio receivers, mobile telephones, radiotelephones,
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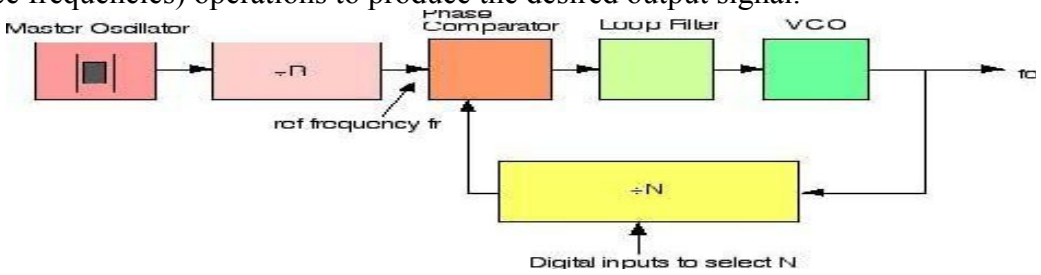
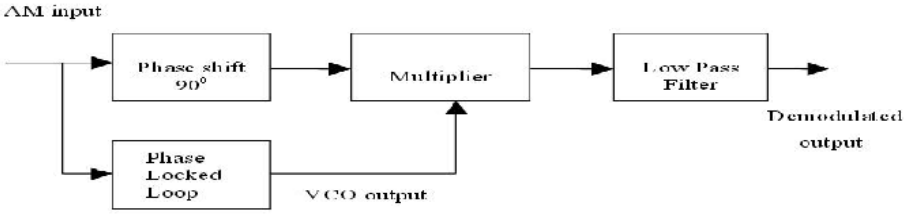


AM demodulator

The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which hasthe same frequency as the carrier, but unmodulated is fed to the multiplier



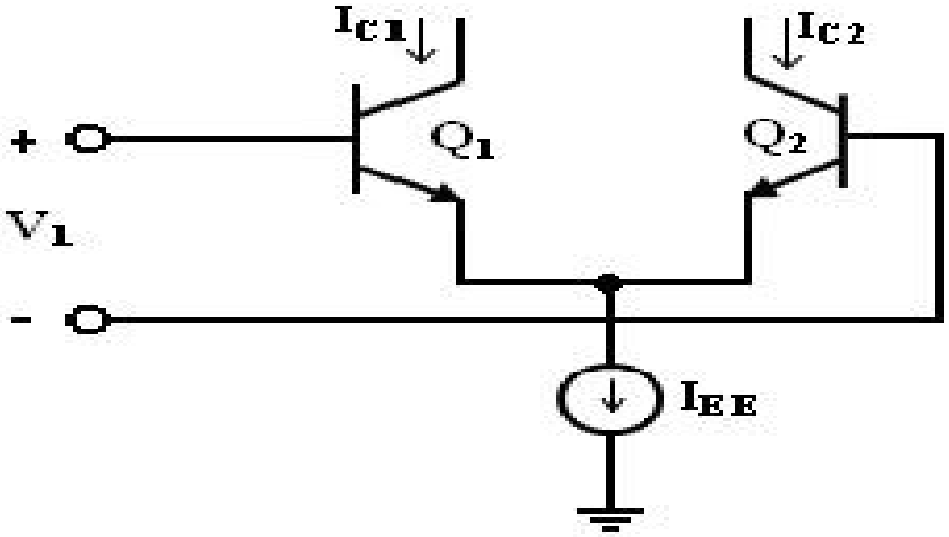
**FM Demodulator **

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.

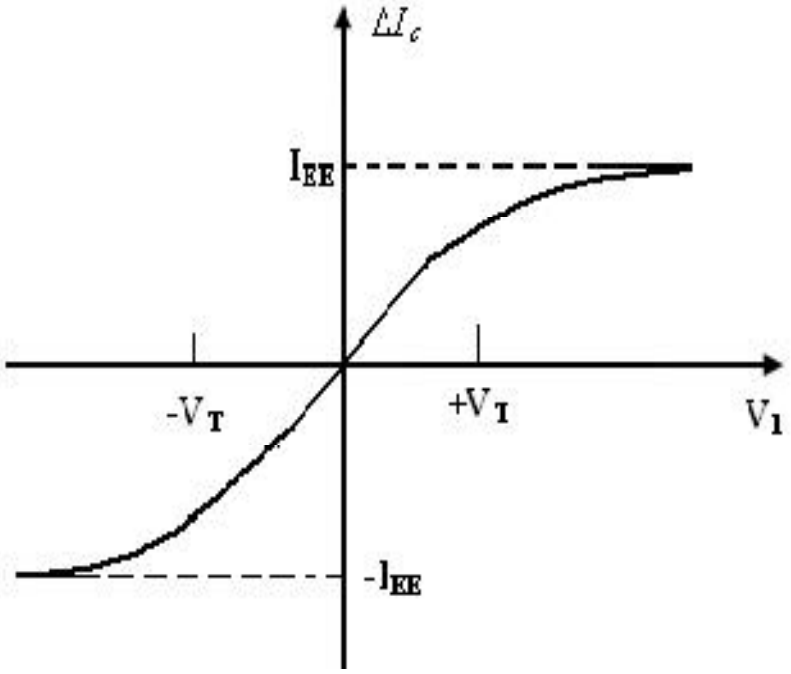
The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM

2. **Explain the working of Analog multiplier using Emitter coupled Transistor Pair. Discuss the Analog Multiplier IC(16)APR/MAY2015 ,(16) MAY/JUNE 2014**

A multiple produces an output V0 which is proportional to the product of two inputs Vx and Vy. V0 = KVxVy where K is the scaling factor = (1/10) V-1.

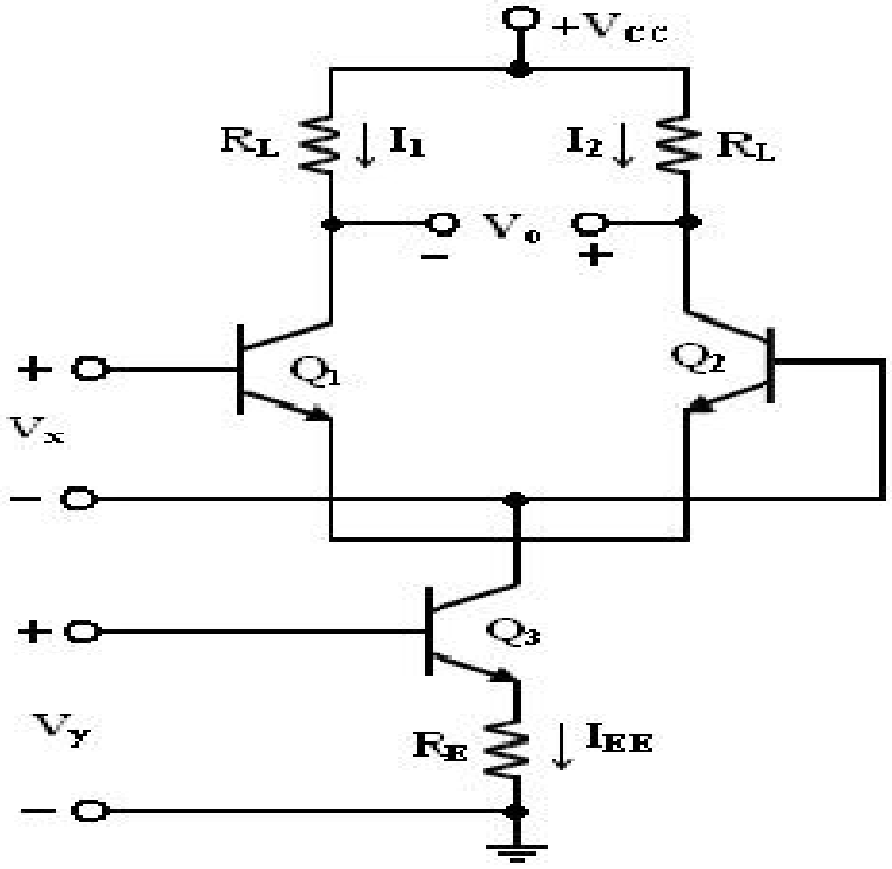


Multiplier circuit using an emitter coupled pair



DC Transfer characteristics of emitter coupled pair

3. Explain the operation of Variable Transconductance Multiplier(16)NOV/DEC2016 MAY/JUNE 2013 (8) MAY/JUNE 2013



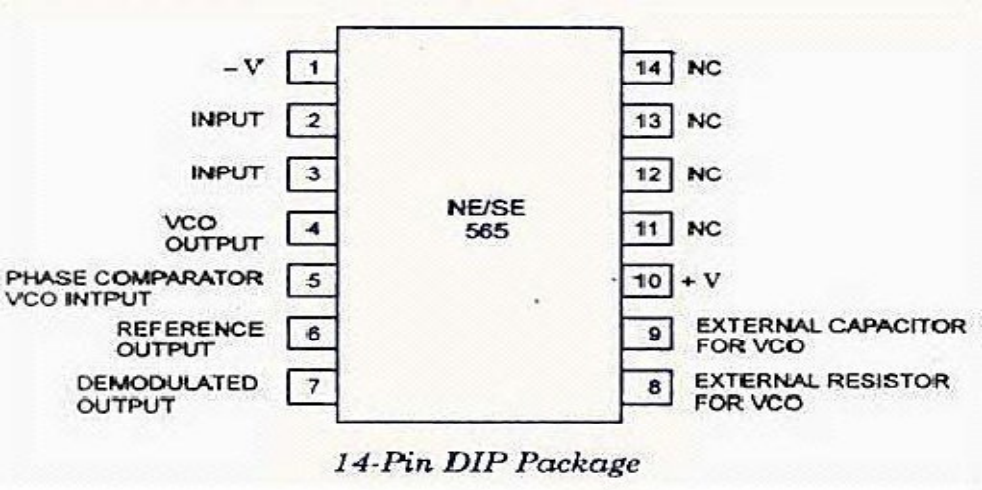
The variable transconductance technique makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. A simple differential circuit arrangement depicting the principle is shown in figure.

- The relationship between V0 and Vx . is given by V0 = gm RL VX where gm = IEE /VT is the transconductance of the stage.
- Application of a second input Vy to the reference current source of the differential amplifier can vary gm.
- Thus, if RE IEE >>VBE, the bias voltage Vy is related to IEE by the relation Vy = IEE RE.
- Then, the overall voltage transfer expression is given by

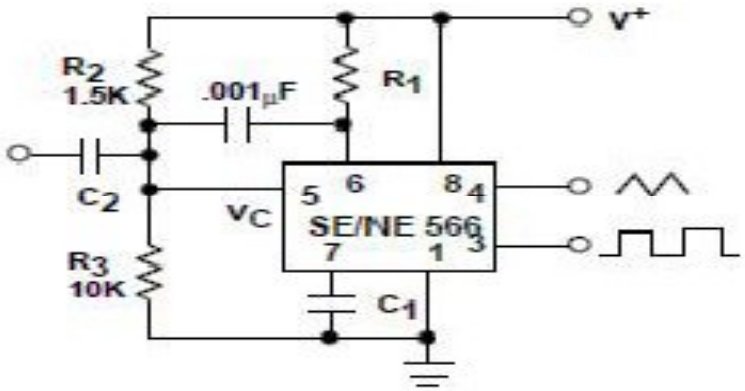
V_O= gm RLVx = (Vy/VTRE)VxRL = VxVy RL/ VTRE

4. (i) Explain working principle of PLL IC NE 565(12) NOV/DEC2016, APR/MAY2017(6) ,NOV/DEC2013 (10)

The output from a PLL system can be obtained either as the voltage signal vc(t) corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator applications whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.



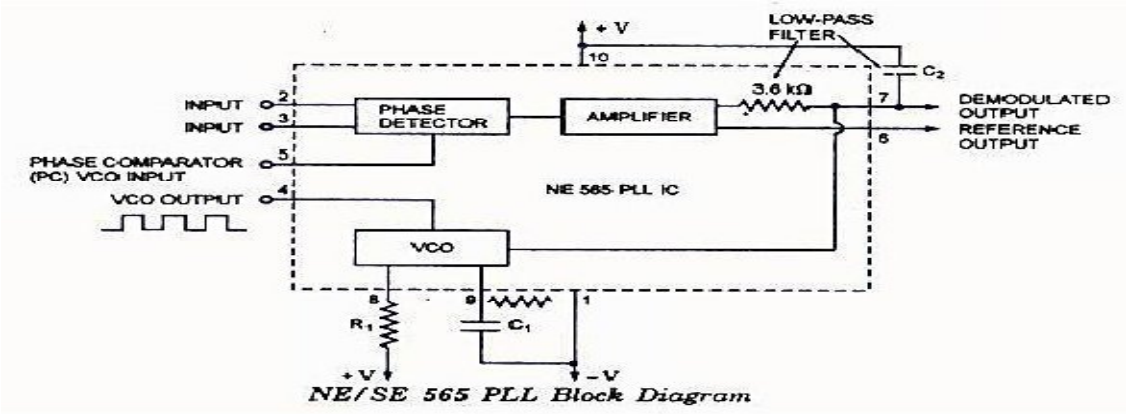
14-Pin DIP Package



The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

External connections of VCO



NE/SE 565 PLL Block Diagram

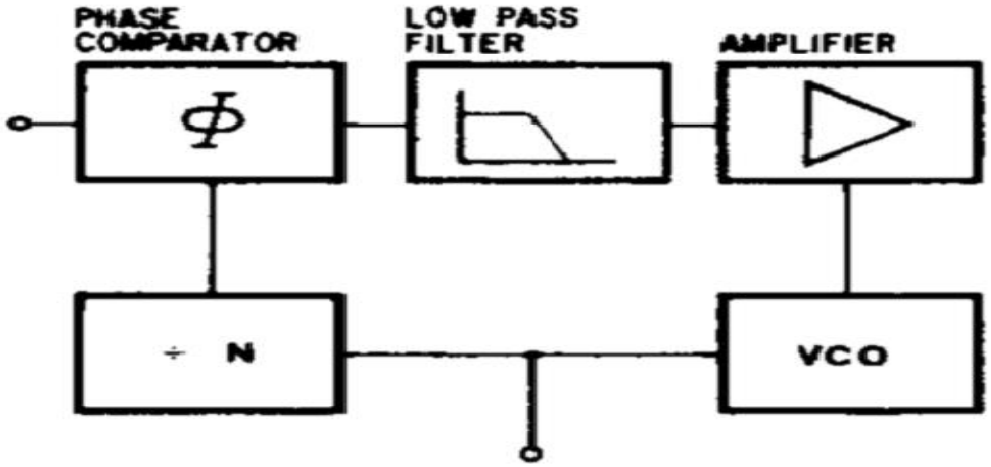
The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$F_{OUT} = 1.2/ 4R_1C_1$

(ii)Brief the application of PLL IC for Frequency Multiplication NOV/DEC2016 (4), APR/MAY2017 (6)

The block diagram shown below shows a frequency multiplier/divider using PLL. A divide by N network is inserter between the VCO output and the phase comparator input. In the locked state, the VCO output frequency fo is given by fo = Nfs. The multiplication factor can be obtained by selecting a proper scaling factor N of the counter. Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. typically n is kept less than 10.

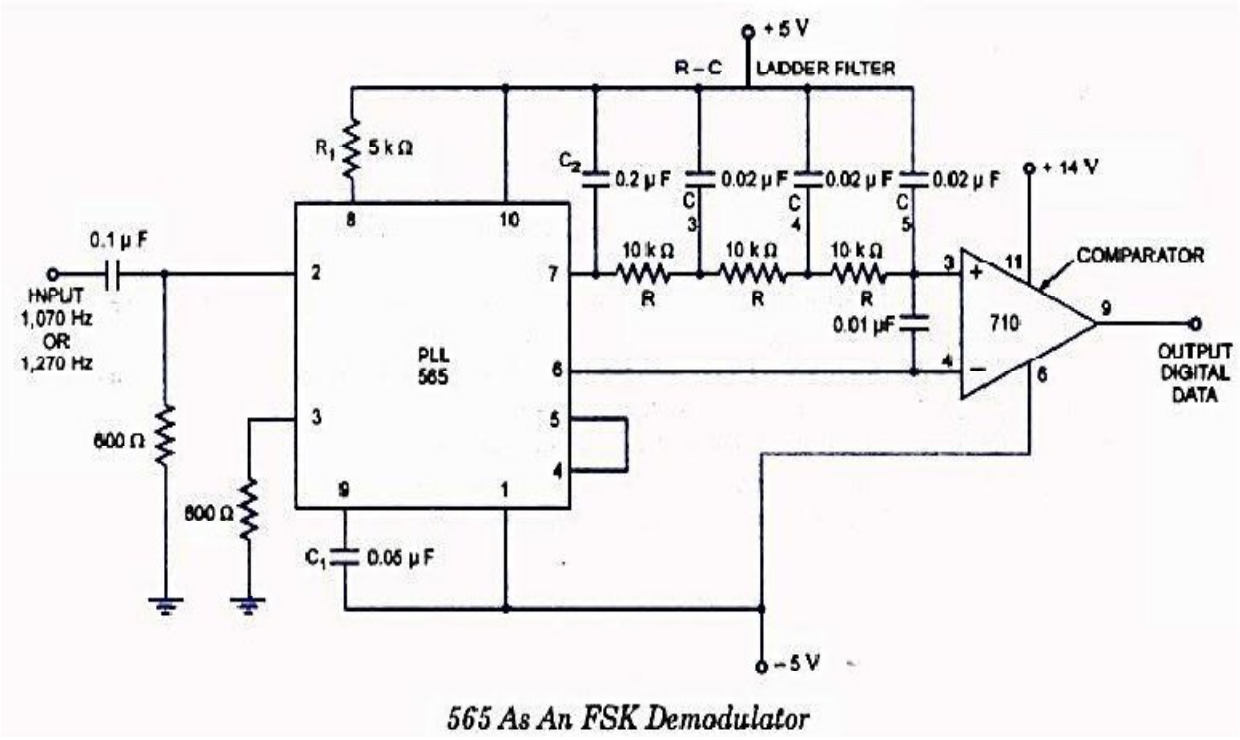


5. Draw the block diagram and explain principle of working, characteristics and applications of (i) Frequency Synthesizer(8) MAY/JUNE 2013, APR/MAY2017 (8)
(ii) FSK demodulator (8) MAY/JUNE 2013

Frequency Shift Keying (FSK) demodulator

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

For example, when transmitting teletype writer information using a modulator-demodulator (modem) a 1070-1270 (mark-space) pair represents the originate signal, while a 2025-2225 Hz (mark-space) pair represents the answer signal.



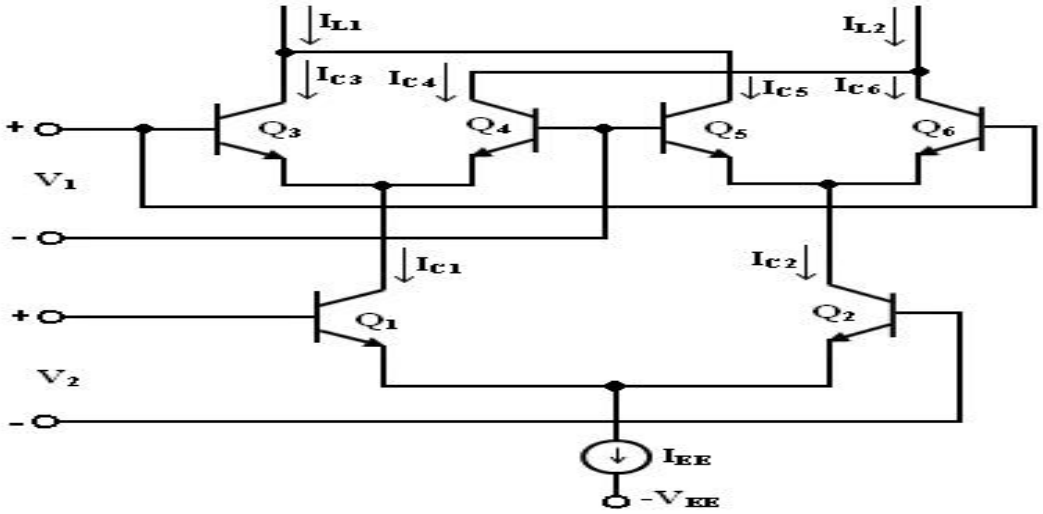
565 As An FSK Demodulator

FSK Demodulator:

- The output of 555 FSK generators is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove dc line.
- At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- R1 & C1 determine the free running frequency of the VCO, 3 stages RC ladder filter is used to remove the carrier component from the output.

6. Explain Gilbert multiplier cell for four quadrant multiplication(7) APR/MAY2017, NOV/DEC2013(11)

The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication



The collector current of Q_3 and Q_4 are given by

$I_{C3}\frac{I_{C1}}{1+e^{-V_1/V_T}}$ and $I_{C4}=\frac{I_{C1}}{1+e^{V_1/V_T}}$

Similarly, the collector current of Q_5 and Q_6 are given by

The $I_{C5}=\frac{I_{C2}}{1+e^{V_1/V_T}}$ and $I_{C6}=\frac{I_{C2}}{1+e^{-V_1/V_T}}$

collector current I_{C1} and I_{C2} of transistors Q_1 and Q_2 can be expressed as

$I_{C1}=\frac{I_{EE}}{1+e^{-V_1/V_T}}$ and $I_{C2}=\frac{I_{EE}}{1+e^{V_2/V_T}}$

Substituting the above equation in I_{C3} and I_{C4}, we get

$$I_{C3}=\frac{I_{EE}}{\left[1+e^{-\frac{V_2}{V_T}}\right]\left[1+e^{-\frac{V_1}{V_T}}\right]} \text{ and } I_{C4}=\frac{I_{EE}}{\left[1+e^{-\frac{V_2}{V_T}}\right]\left[1+e^{\frac{V_1}{V_T}}\right]}$$

Similarly substituting I_{c2} in I_{c5} and I_{C6}, we get,

$$I_{C5}=\frac{I_{EE}}{\left[1+e^{\frac{V_2}{V_T}}\right]\left[1+e^{\frac{V_1}{V_T}}\right]} \text{ and } I_{C6}=\frac{I_{EE}}{\left[1+e^{\frac{V_2}{V_T}}\right]\left[1+e^{-\frac{V_1}{V_T}}\right]}$$

The differential output current I is given by

I =I L1 - I L2

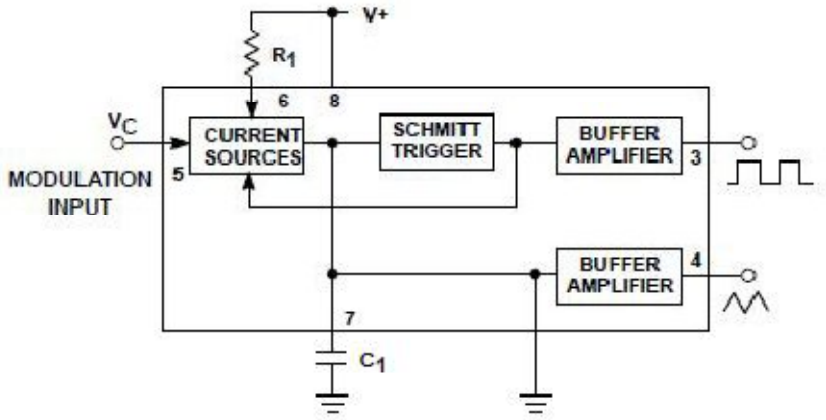
= IC3 +IC5) - (IC4+IC6)

=IC3 - IC6)-(IC4 - IC5)

ΔI=I EE tanh(V1/2VT) tanh(V2/2VT)

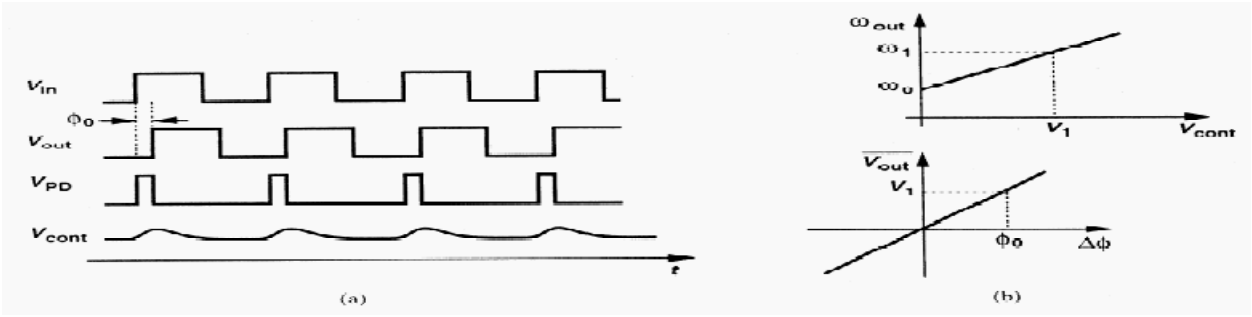
7. Explain operation of VCO (6) APR/MAY2017 , (10) NOV/DEC 2012,

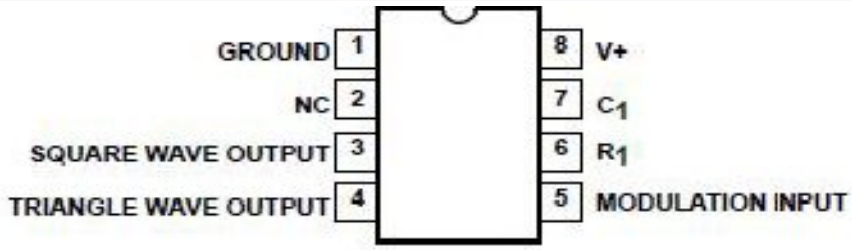
In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.



The VCO oscillates at an angular frequency, ωout. Its frequency is set to a nominal ω0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient KO or KVCO (rad/s/v).

$\omega out = \omega 0 + KOVcont$





The output frequency of the VCO can be given as follows:

$$f_o = \frac{2\,[(V+) - (V_C)]}{R_1\, C_1\, V+}$$

8. (i) List and define the various performance parameters of a Multiplier IC. (6)

Accuracy:

This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.

Linearity:

This defines the accuracy of the multiplier. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.

✓ **Square law accuracy:**

The Square – law curve is obtained with the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square –law curve expresses the squaring mode accuracy.

Bandwidth:

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values.

✓ **Quadrant:**

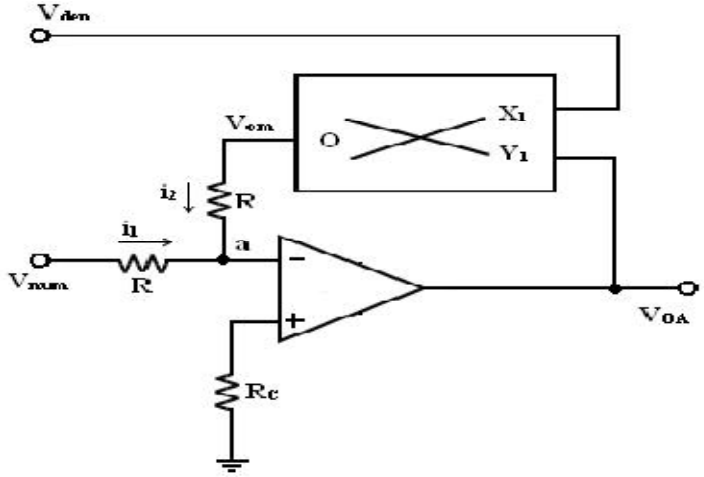
The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

✓ **Logarithmic summing Technique:**

This technique uses the relationship lnVx + lnVy =ln(VxVy)

(ii) How the multiplier is used as voltage divider? (5)

In voltage divider circuit the division is achieved by connecting the multiplier in the feedback loop of an op-amp.



$i1+i2 = Vnum / R + Vom /R = 0$

KV OA V den = - V num or

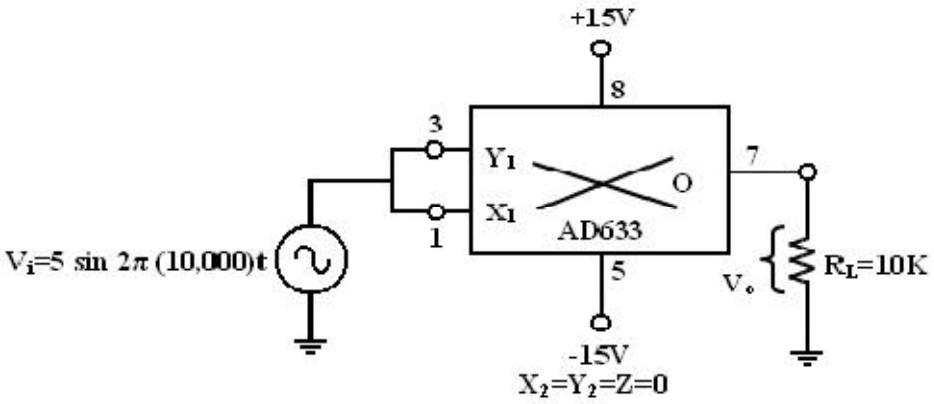
voA=- vnum/Kvden

(iii) How the multiplier is used as frequency doubler? (5) MAY/JUNE2012

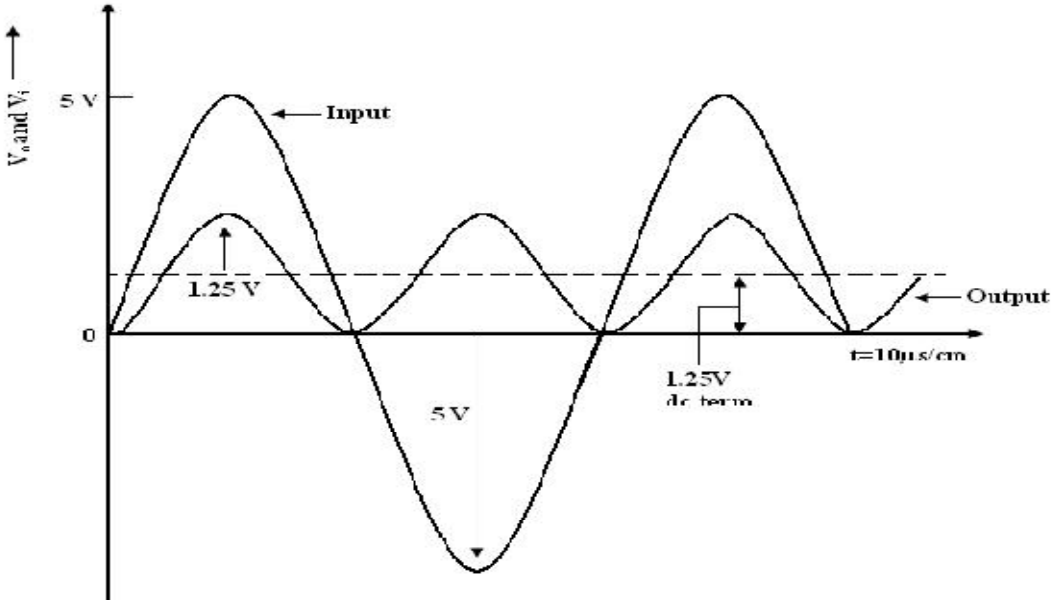
The principle of application of analog multiplier as rectifier of ac signals.

A sine-wave signal Vi has a peak amplitude of Av and frequency of f Hz. Then, the output voltage of the doublers circuit is given by

$$v_0 = \frac{A_v \sin 2\pi ft * A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10} \sin^2 2\pi ft = \frac{A_v^2}{20}(1 - \cos 4\pi ft)$$



(a) circuit diagram



(b) input –output waveform of frequency doubler

9. Explain the basic blocks of PLL and determine expression for lock- in range and capture range APR/MAY2015(16), NOV/DEC 2015(16)

Definition

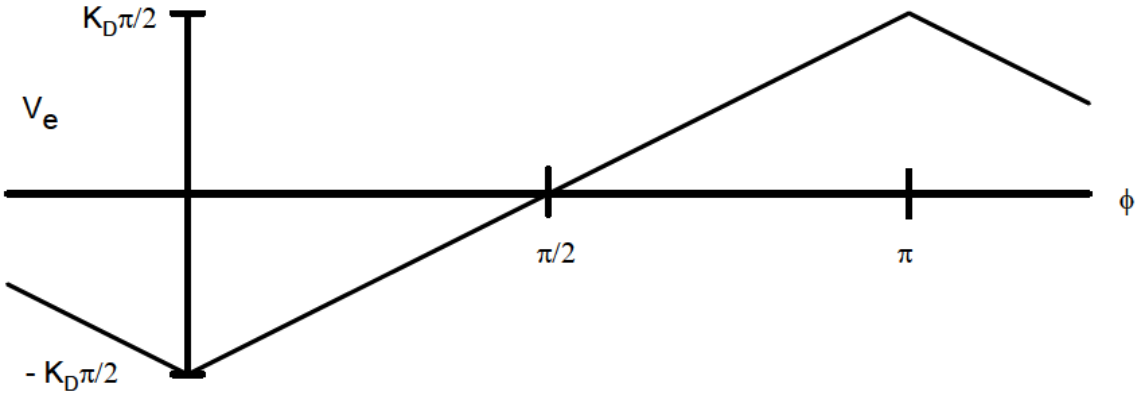
A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

Applications: There are many applications for the PLL, but we will study:

a. Clock generation
b. Frequency synthesizer
c. Clock recovery in a serial data link

Lock Range

Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.



Thus the frequency would change in the opposite direction to that required to maintain the locked condition.

$$Ve\text{-}max = \pm KD\ \pi/2$$

When the phase detector output voltage is applied through the loop filter to the VCO,

$$\Delta\omega out - max = \pm KV\ \pi/2 = \omega L \text{ (lock range)}$$

Where KV = KO KD, the product of the phase detector and VCO gains.

Capture range:

Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detecto is added to the phase detector to assist in initial acquisition of lock. You will see later that the loop filter bandwidth has an effect on the capture range.

$$Ve(s)/\Delta\varphi = KD$$
$$\varphi out(s)/Vcont(s) = KO/s$$

UNIT 4 (2 MARKS)

1. Give the advantages of integrating type ADC. APRIL/MAY 2010

- The integrating type of ADC's does not need a sample/Hold circuit at the input.
- It is possible to transmit frequency even in noisy environment or in an isolated form.

2. Compare and contrast binary ladder and R-2R ladder DAC? NOV/DEC 2010

Binary ladder	R-2R ladder
1. Requirement of wide range of resister values. 2. As the length of the binary word is increased .the range of resister values needed also increases.	1. Easier to build accurately as only two precision metal films are required. 2. Number of bits can be expanded by adding more sections of same R/2R values.

3. **Define resolution and conversion time of DAC. NOV/DEC 2010**

Conversion Time

It is defined as the total time required to convert digital signal into its analog output.

Resolution

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

Resolution (in volts)= $V_{OFS}/2^n-1$

4. **Define settling time of D/A converter. MAY/ JUNE 2012**

It represents the time it takes for the output to settle within a specified band ±½LSB of its final value following a code change at the input (usually a full scale change).

5. What is the main drawback of dual slope ADC? MAY/ JUNE 2012

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC.

6. What is a sample/hold circuit? APRIL/MAY 2014

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

7. **Define settling time of D/A converter? MAY/ JUNE 2012**

It represents the time it takes for the output to settle within a specified band LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitance & inductances. Settling time ranges from 100ns. 10μ s depending on word length & type circuit used.

8. **Define accuracy of D/A converter. APRIL/MAY 2011**

Absolute accuracy:

It is the maximum deviation between the actual converter output & the ideal converter output.

Relative accuracy:

It is the maximum deviation after gain & offset errors have been removed.

The accuracy of a converter is also specified in form of LSB increments or % of full scale voltage.

9. **What is the main drawback of a dual-slop ADC? MAY/ JUNE 2012**

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC.

10. **Which is the fastest ADC and why? MAY/ JUNE 2010**

Simultaneous type A/D converter (flash type A/D converter) is the fastest because A/D conversion is performed simultaneously through a set of comparators

UNIT –IV (16 MARKS)

1. **(i)How are A/D converters categorized (6) APRIL/MAY2017**

Classified based on their operational Features

Type-1: the A/D converters can be classified into two Groups as

(a) Programmed A/D converters
(b) Non Programmed A/D converters

Type-2: the A/D converters can be classified into two Groups as

(c) Closed loop or feedback type A/D converters
(d) Open –loop type A/D converters

Type-3: the A/D converters can be classified into two Groups as

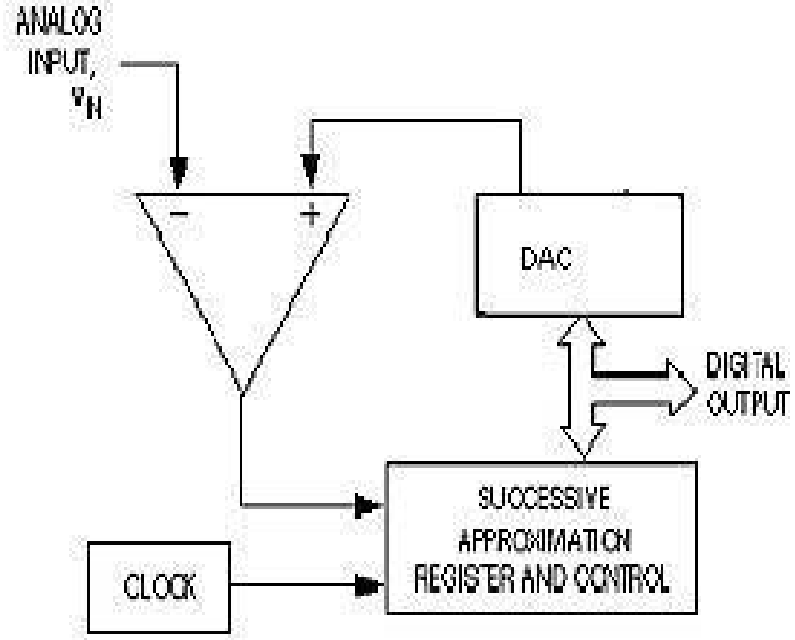
(e) Capacitor-charging type A/D converters
(f) Discrete Voltage comparison type A/D converters

Type-4: the A/D converters can be classified into two Groups based on their conversion techniques as

(g) Direct type A/D converters
(h) Integrating type A/D converters

(ii)Discuss on successive approximation type DAC (7) APRIL/MAY2017, NOV/DEC2015 (16), and NOV/DEC2013 (10) , NOV/DEC2012 (8), APR/MAY 2011(8), APR/MAY2010 (8), NOV/DEC 2010 (8)

Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC).



2. (i)What is meant by resolution , offset Error in DAC(6) APRIL/MAY2017

Resolution

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = VoFS / (2 n - 1) = 1 LSB increment

Where

'n' is the number of input bits

'VoFS' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

Offset Error

The simplest Kind of static Errors are Offset Error and Gain error.

Ideally, the output of a D/A converter is 0v when all the bits of binary input word are 0's. in practice ,however there is a very small output voltage called offset voltage or offset error

(ii)Discuss on the dual slope type ADC (7) APRIL/MAY2017, APR/MAY2014 (16), NOV/DEC2013 (10), MAY/JUNE 2012(10) ,NOV/DEC 2010 (8), APR/MAY 2008 (8), APR/MAY 2006 (8)

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again.

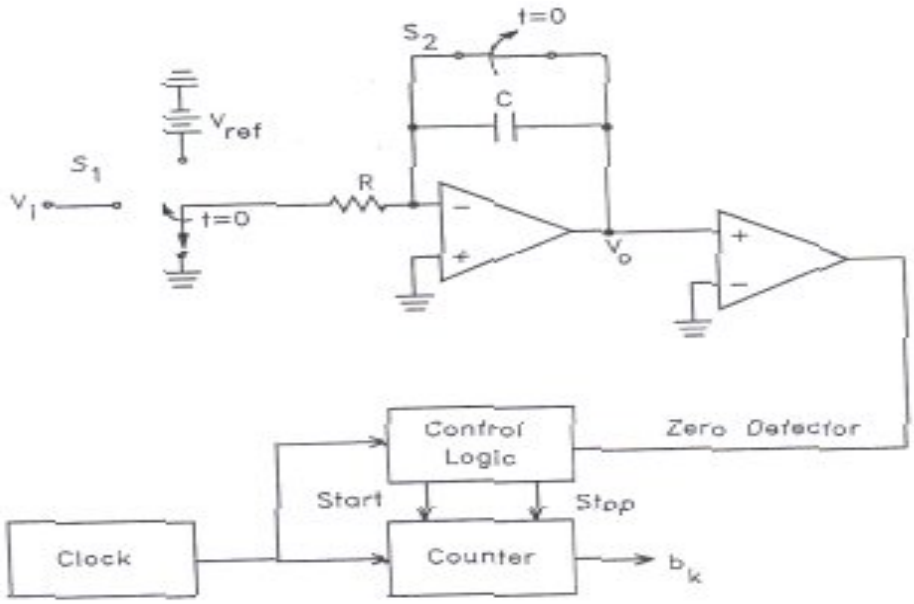
The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

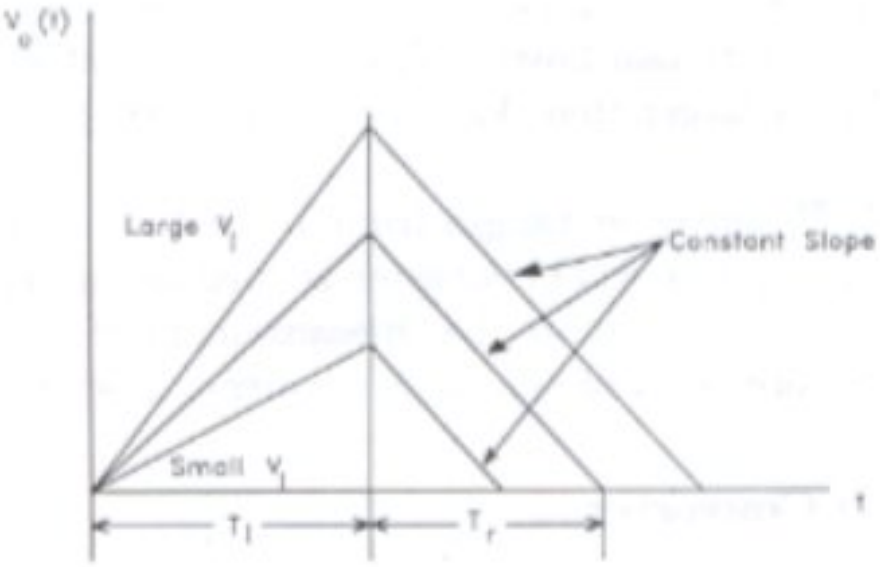
An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period).

The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period.

The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution.

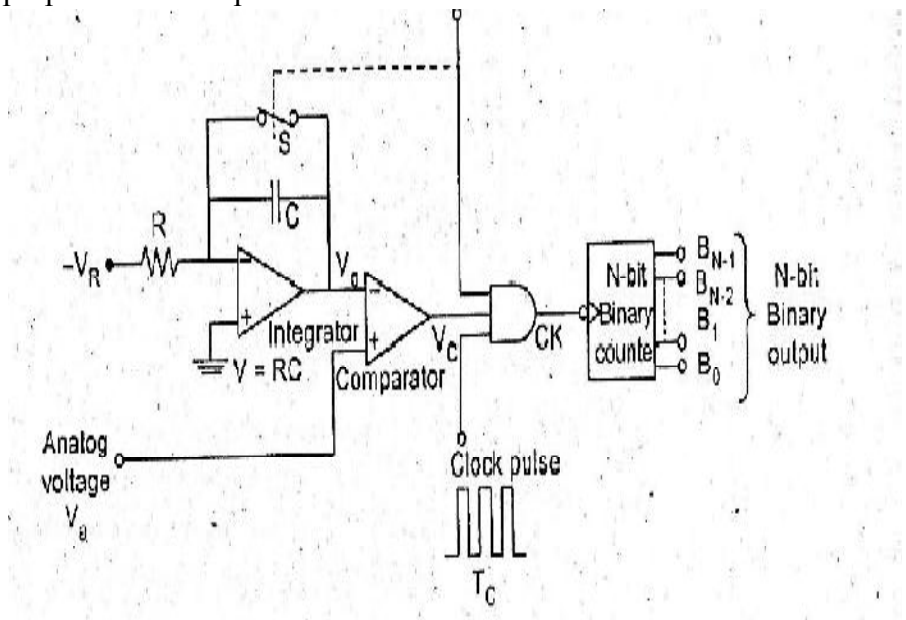
Use: Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.



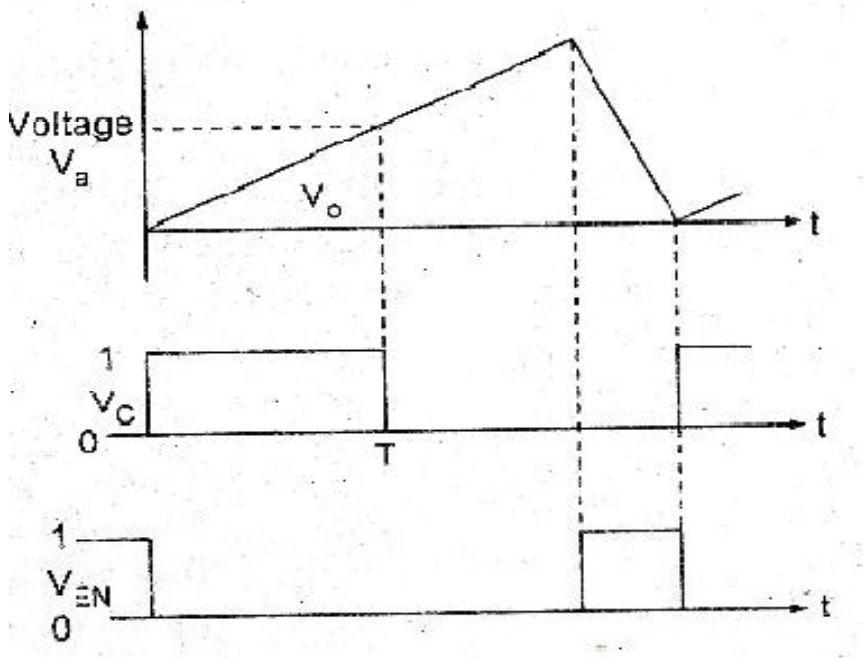


3. With functional block diagram Explain voltage to time converter with input and output waveform (16) NOV/DEC2016

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period

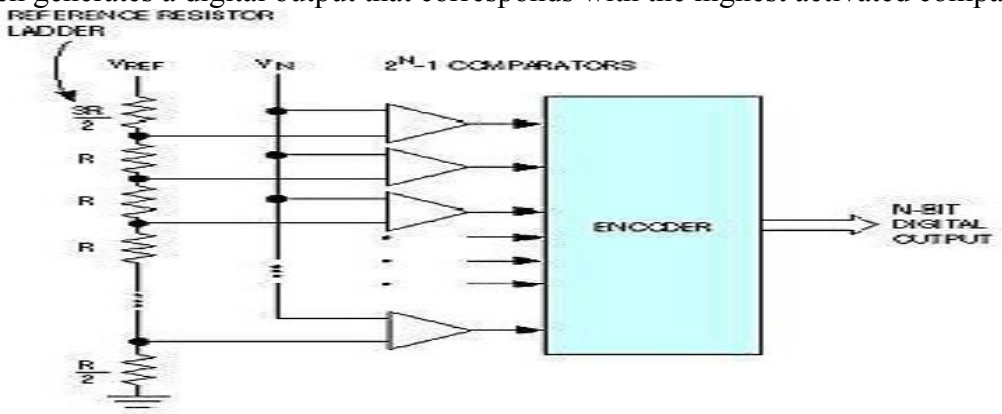


Conversion process



4. (i)Explain the Flash type ADC. what are its merits and demerits(10) APRIL/MAY2017 ,NOV/DEC2016(10), NOV/DEC2015(16), APR/MAY2014(10), NOV/DEC2011(8), MAY/JUNE 2007 (8)

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator



Merits

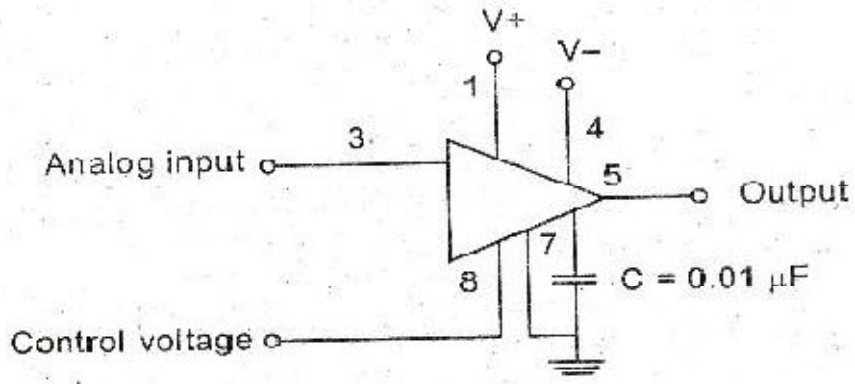
Fastest ADC because performed simultaneously through a set of comparators
Construction is simple and easier to design

Demerits

Not suitable for more than 3 or 4 digital output bits

(ii) Write a note on high speed sample and hold circuits (6) APR/MAY2017, NOV/DEC2011 (8), APR/MAY 2010 (8), NOV/DEC 2010 (8)

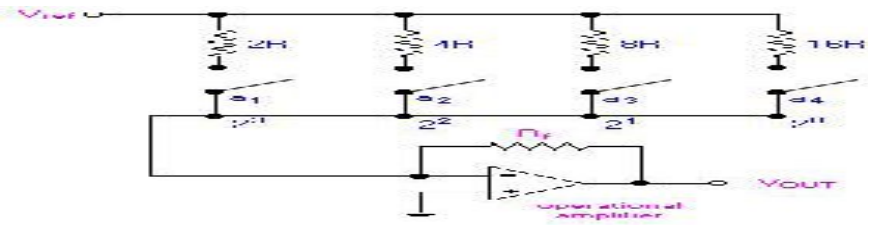
During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP.



Three S/H circuits to reduce error:

- o series sampling,
- o SOP based S/H circuit,
- o bottom plate S/H circuit with bootstrapped switch

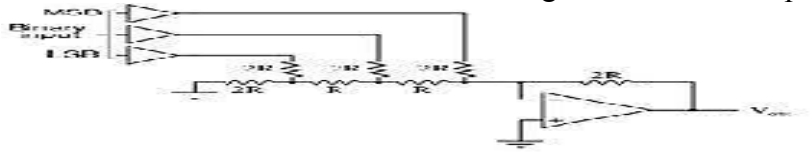
5. Explain weighted resistor type and R-2R Ladder type DAC APR/MAY2014 Binary-Weighted Resistor DAC NOV/DEC2013 (6), NOV/DEC2012 (6), APR/MAY 2011(8), APR/MAY 2008 (8), APR/MAY 2006 (8)



$$V_{OUT} = -iR_f$$
$$= -\left[V_{ref}\left(\frac{a_1}{2R} + \frac{a_2}{4R} + \frac{a_3}{8R} + \frac{a_4}{16R}\right)\right]R_f$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16}\right)$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1} + \frac{a_2}{2^2} + \frac{a_3}{2^3} + \frac{a_4}{2^4}\right)$$

R-2R Ladder DAC APR/MAY2014, NOV/DEC2013 (6), NOV/DEC2012 (5), APR/MAY 2011(8) , APR/MAY2010(8), NOV/DEC 2010 (8),MAY/JUNE 2007 (8)

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages.



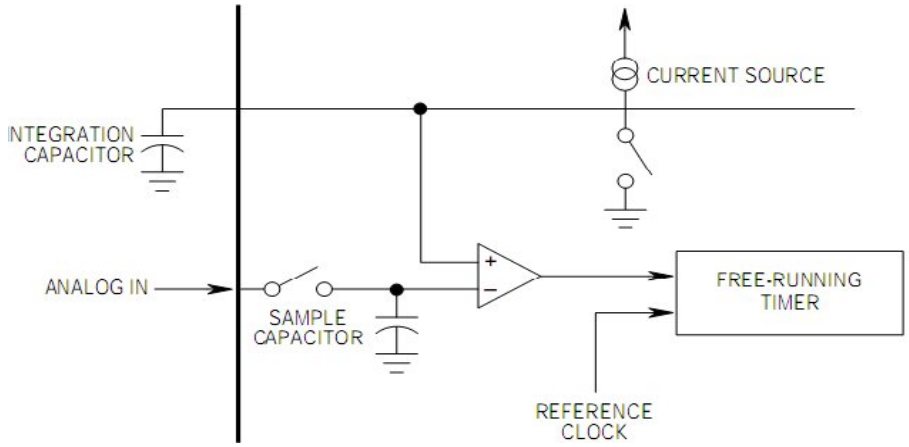
operation of a R-2R ladder DAC

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V
110	-7.50 V
111	-8.75 V |.

6. Explain Flash type, Single type and Dual slope type ADC. APR/MAY2014

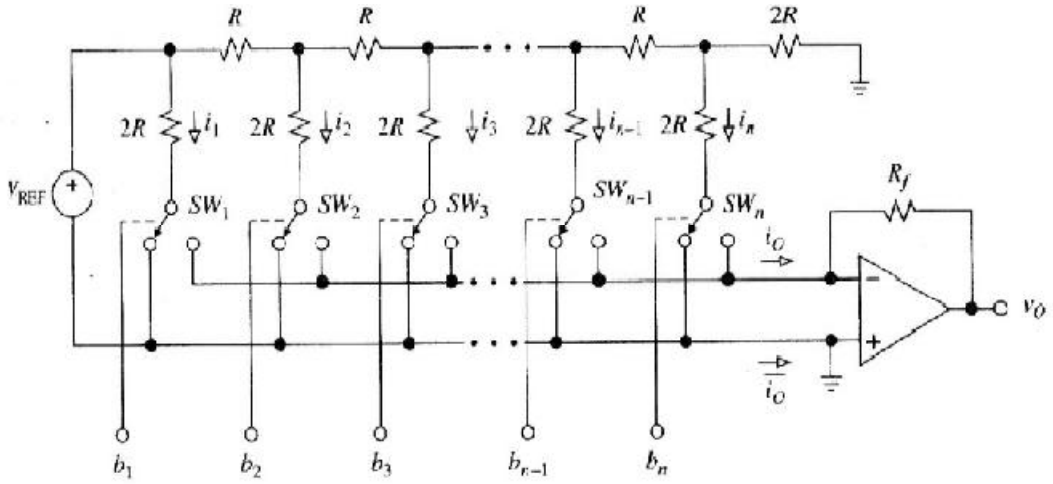
Single type

The main circuit of this converter is a ramp generator, which on receiving a RESET from the control circuit increases linearly with time from 0v to a maximum voltage V_m



7. (i) With circuit explain current mode type of DACs. Compare with voltage mode type (10) APR/MAY 2015

Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into *i*1 , *i*2, *i*3 ……*i*n. in each arm. The currents are either diverted to the ground bus (*io*) or to the Virtual-ground bus *(io*).



V0 = - (Rf/R) VREF (b12-1 + b22-2+ …….. + bn2-n)

Compare with voltage mode type

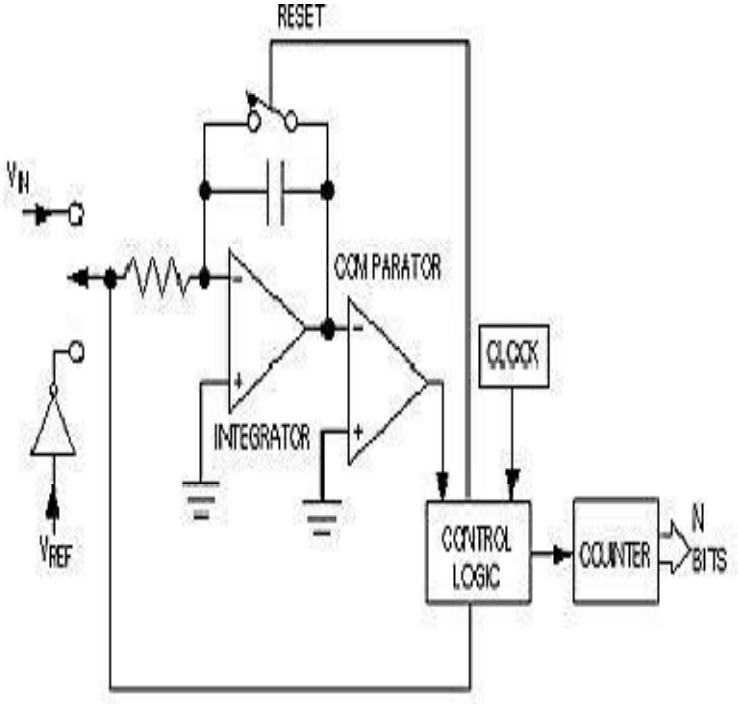
1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.
2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the

Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

3. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.
4. More accurate selection and design of resistors R and 2R are possible and simple construction.
5. The binary word length can be easily increased by adding the required number or R-2R sections.

(ii) What are oversampling Data Converters?(6) APR/MAY2015, NOV/DEC2012(8), APR/MAY 2011(8)

It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, Low noise and low cost. Typical applications are for speech and audio.



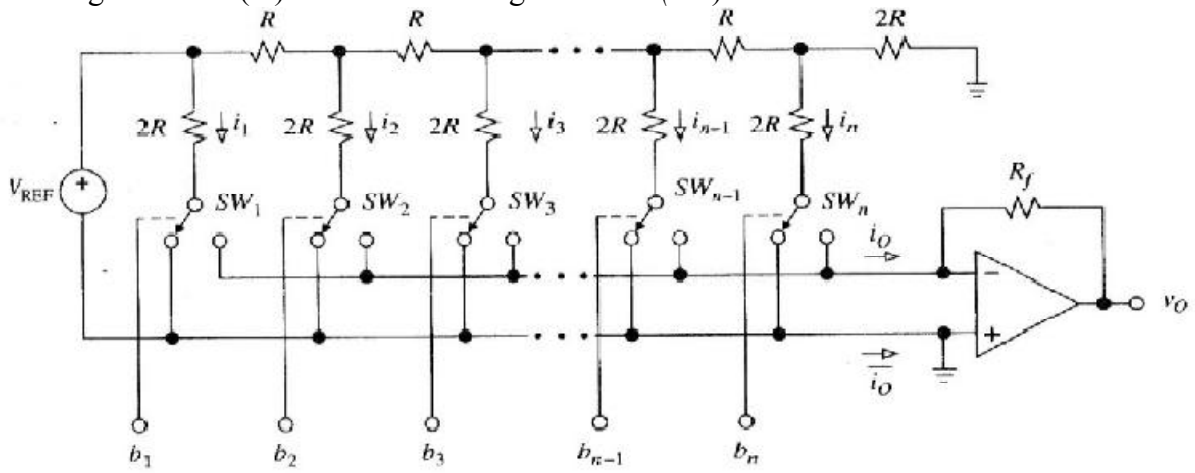
8. Explain the following types of DAC with suitable diagrams NOV/DEC2012, NOV/DEC2011

(i)Binary-Weighted Resistor DAC (6)

(ii)R-2R Ladder DAC(5)

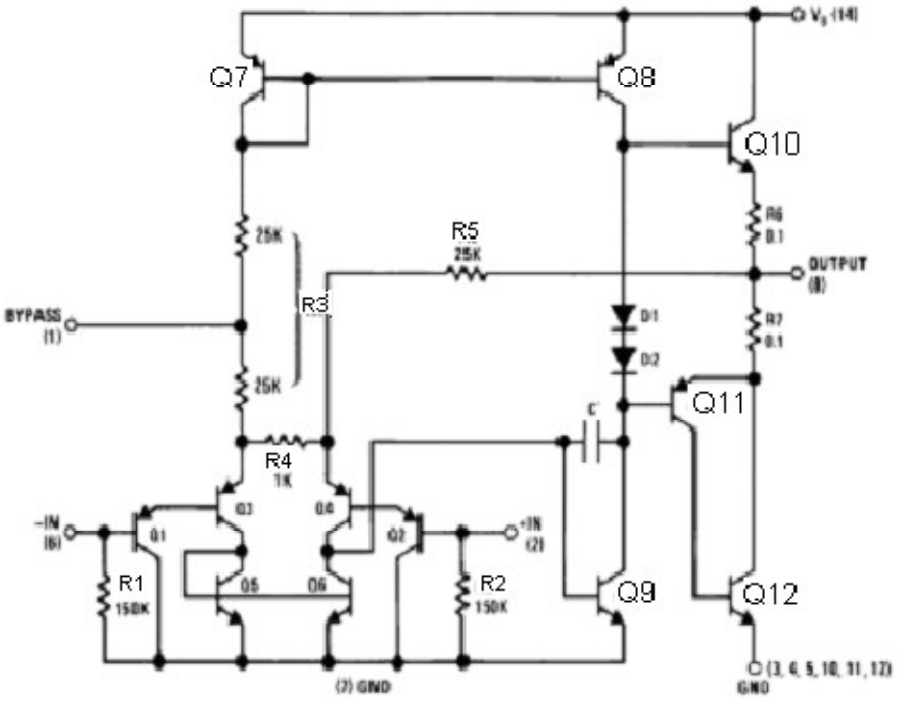
(iii) inverted R-2R ladder DAC(5)

Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into *i*1 , *i*2, *i*3 ……*i*n. in each arm. The currents are either diverted to the ground bus (*io*) or to the Virtual-ground bus *(io*).



UNIT 5 (2 MARKS)

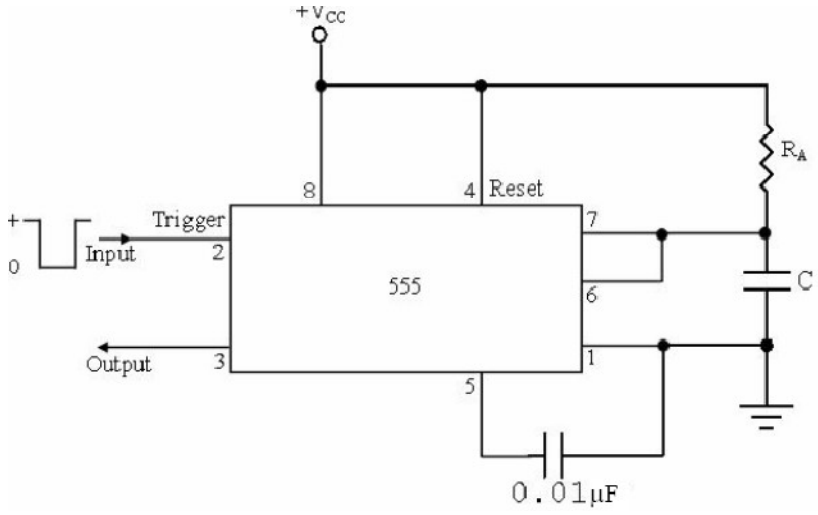
1. **Draw the internal circuit for audio power amplifier APRIL/MAY 2010**



2. **What are the three different wave forms generated by ICL8038? APRIL/MAY 2010**

Sine-wave generators, square wave generator, Triangular wave generator and saw-tooth wave generator.

3. **Sketch the monostable multivibrator circuit diagram using 1C555. NOV/DEC 2010**



4. **What is meant by thermal shutdown applied to voltage regulators? NOV/DEC 2010**

Thermal Shutdown means that the chip will automatically itself OFF if the internal temperature exceeds typically 175^0C.

5. **What is an opto-coupler? APRIL/MAY 2014**

An opto-isolator, also called an optocoupler, photocoupler, or optical isolator Opto-coupler IC is a combined package of a photo-emitting device and a photosensing device.

Examples for opto-coupler circuit :

LED and a photo diode, LED and photo transistor, LED and Darlington,

Examples for opto-coupler IC :

MCT 2F , MCT 2E .

6. **List the two type of multivibrators. APRIL/MAY 2014**

Astable Multivibrators

Monostable Multivibrators

7. **Define the duty cucle in Astable multivibrator IC555 APRIL/MAY 2011**

It is defined as the ratio of on time to the total time of one cycle.

D = W/ T

W – time for output is high = TON

T – total time of one cycle.

8. **Give the formula for period of oscillation in an OP-AMP astable circuit MAY/JUNE 2013**

T = 0.693 (RA + 2 RB) C seconds

9. **State the applications of 555 Timer IC NOV/DEC 2013**

- Oscillator
- Pulse generator
- Ramp and square wave generator
- Mono-shot multivibrator
- Burglar alarm
- Traffic light control.

10. **What are the three different wave forms generated by ICL8038? APRIL/MAY 2010**

- Triangular wave
- Sine wave
- Square Wave

UNIT 5 (16 MARKS)

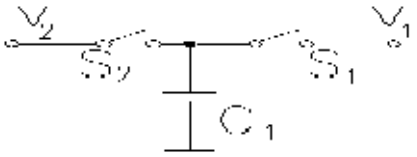
1. **Answer any two of the following APR/MAY 2017(6+7)**
   - **(i) Switched capacitor Filter APR/MAY2011(8), NOV/DEC2011(8)**
   - **(ii) Audio power Amplifier**
   - **(iii) Opto coupler APR/MAY 2017(6+7) , NOV/DEC2013(2), MAY/JUNE2012(8)**

(i)Switched Capacitor Filter

The switched capacitor filter allows for very sophisticated, accurate, and tunable analog circuits to be manufactured without using resistors.

Advantages: resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

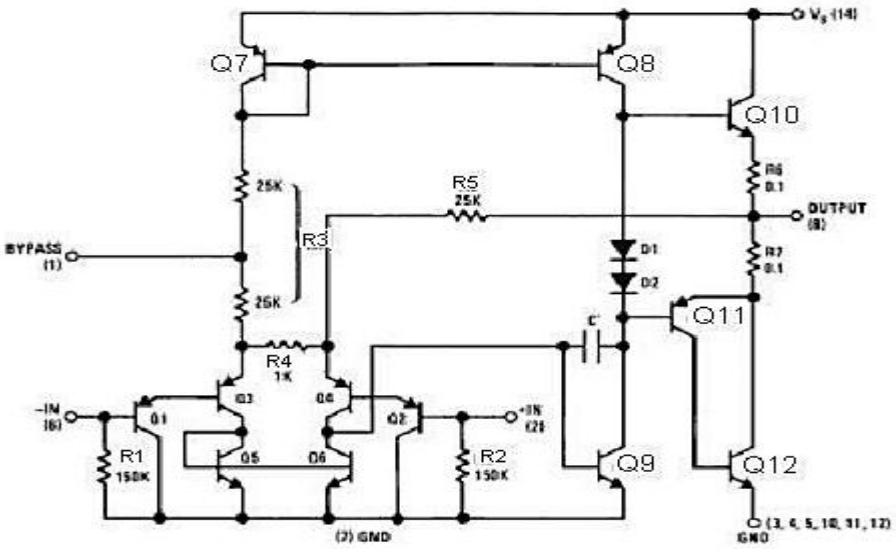
$$\Delta q = C_1(v_2 \quad v_1)$$

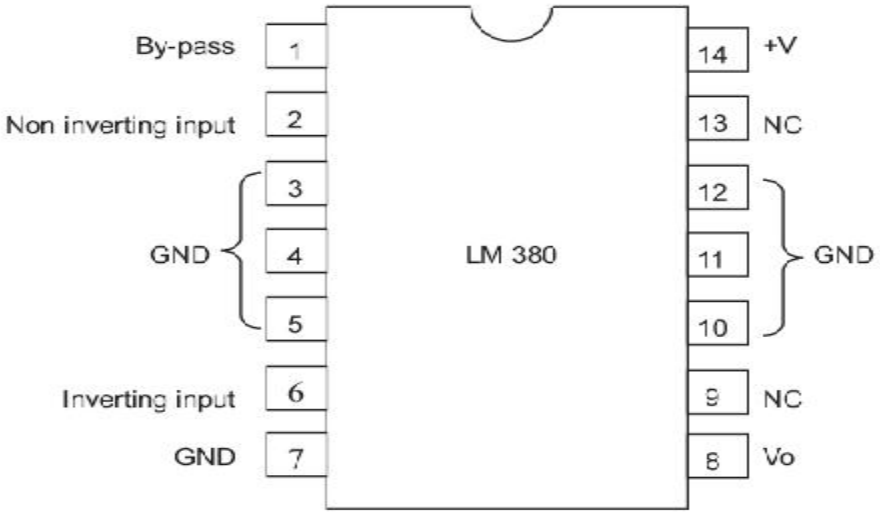


Switched Capacitor Filter ICs:

Some of the Switched capacitor filter ICs is MF 5, MF10 and MF100

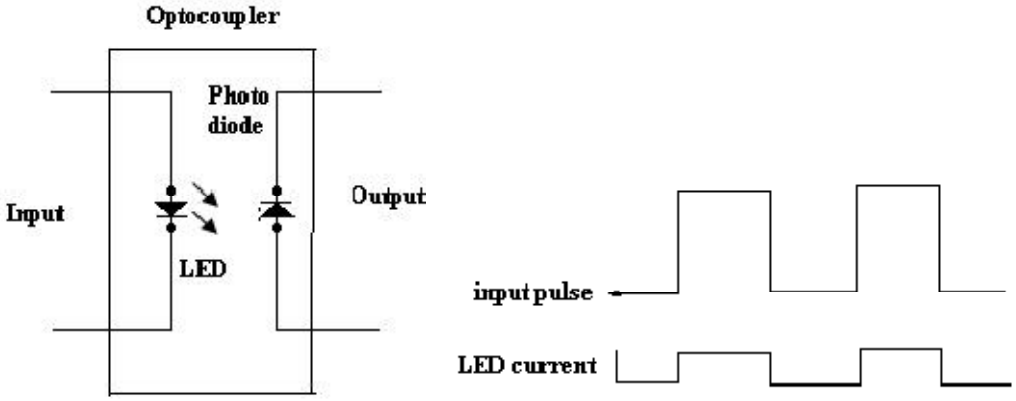
(ii)Audio power Amplifier





LM380 circuit description:
It is connected of 4 stages,
(i) PNP emitter follower
(ii) Different amplifier
(iii) Common emitter
(**iv**)Emitter follower

(iii) Opto coupler



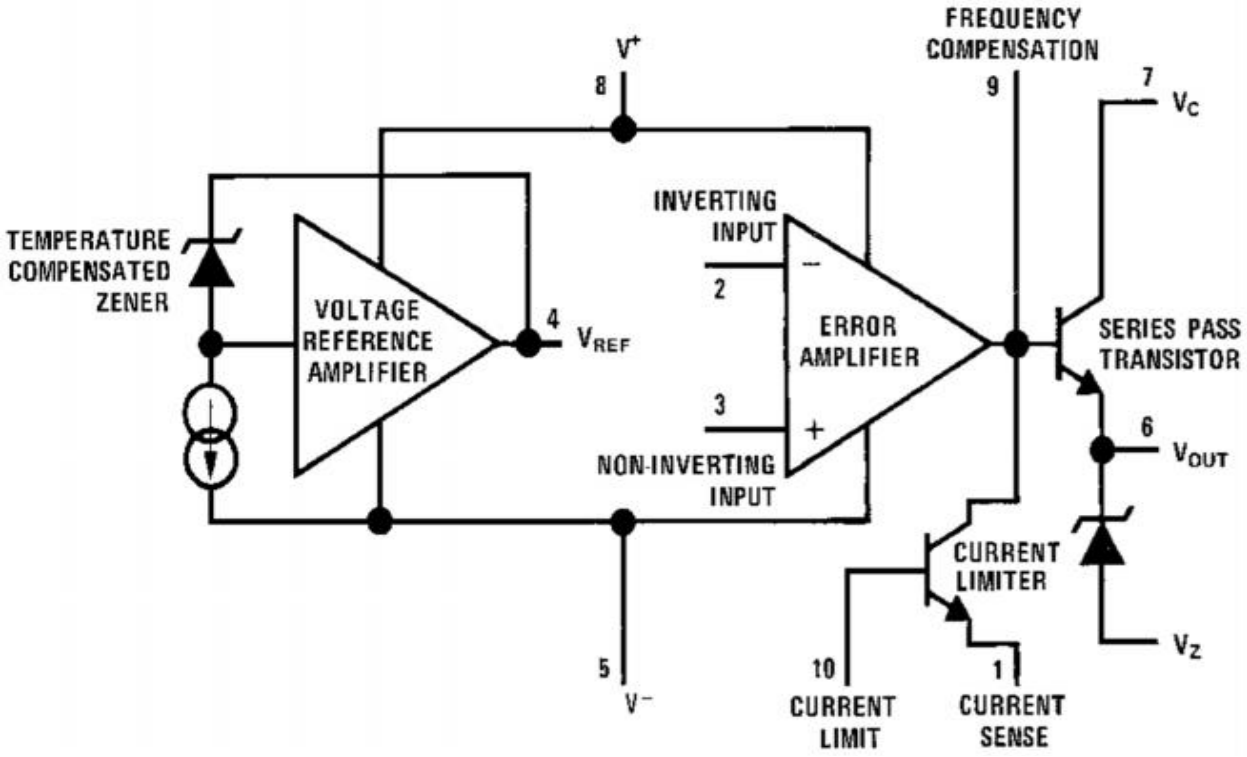
Opto couplers or Opt isolators is a combination of light source & light detector in the same package.

They are used to couple signal from one point to other optically, by providing a complete electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

Characteristics of opto coupler:

(i) Current Transfer Ratio
(ii) Isolation voltage between input & output
(iii) Response Time
(iv) Common mode Rejection

2. (i) How is 723 IC configured as a high voltage regulator circuit? Draw the schematic and explain (8) APR/MAY2015 , (16) APR/MAY2014, MAY/JUNE2012(8)



IC723 as a HIGH voltage LOW Current:

 This circuit is capable of supplying a regulated output voltage between the ranges of 7 to 37 volts with a maximum load current of 150 mA.

 The Non – inverting terminal is now connected to Vref through resistance R3.

 The value of R1 & R2 is adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

Vin = Vref =R2 /(R1+R2) V0

Vo = [1+R1/R2] Vin

 Rsc is connected between CL & Cs terminals as before & it provides the short Circuit current limiting Rsc =0.6/Ilimit

 The value of resistors R3 is given by ,

R3= R1ll R2 =R1R2/(R1+R2)

IC723 as a HIGH voltage HIGH Current:

 An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.

For this circuit the output voltage varies between 7 & 37V.

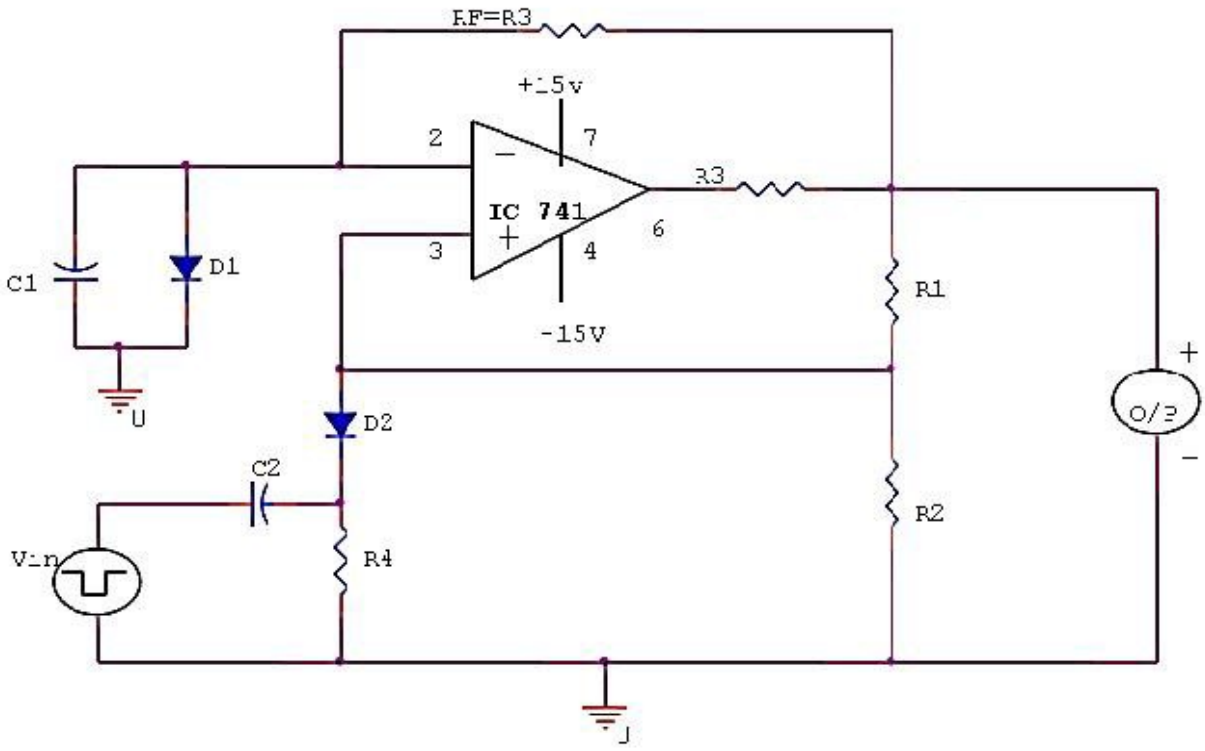
 Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.

 The output voltage Vo is given by ,

V0= Vo = [1+R1/R2] Vin

Rsc =0.6/Ilimit

(ii) Explain the monostable mode operation of IC 555 timer (8) APR/MAY2015, NOV/DEC 2015 (16) , NOV/DEC2013(10)



Design:

1. Calculating β from expression

$$\beta = \frac{R1}{R1 + R2}$$

2. The value of R & C from the pulse width time expression.

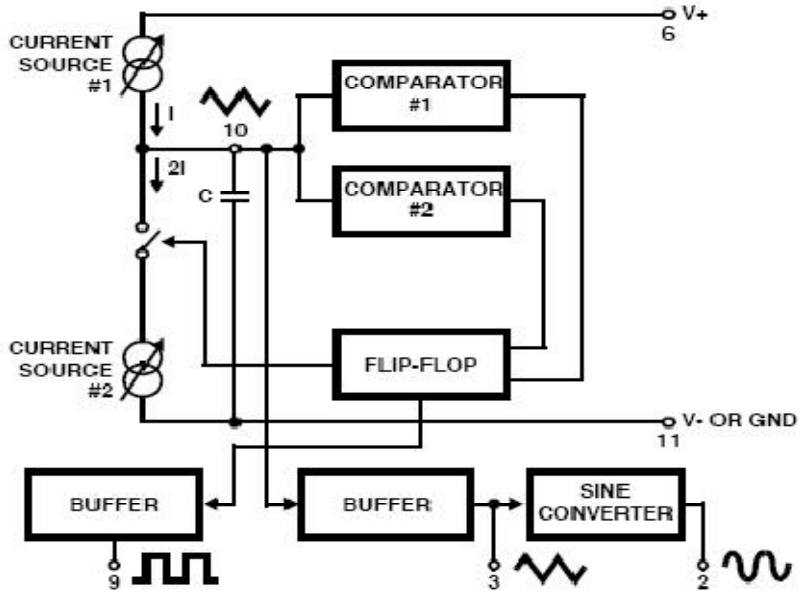
$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta}$$

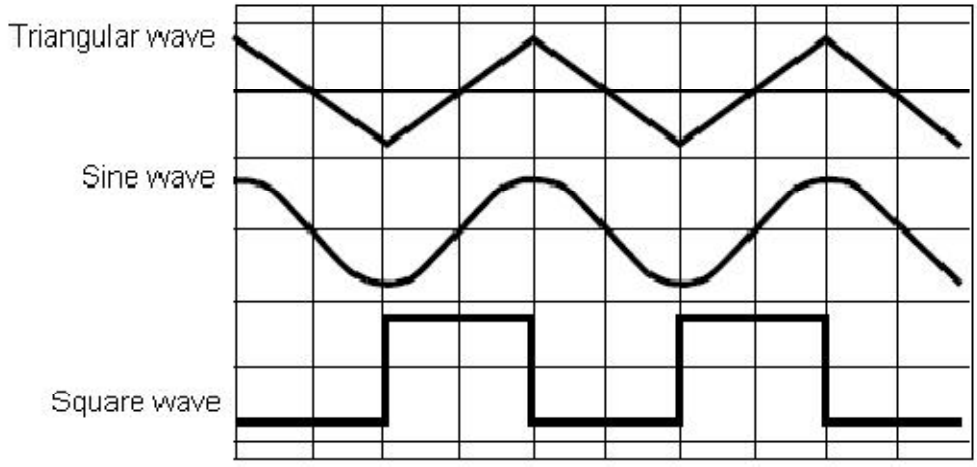
$$T = RC \ln \frac{(1 + V_D / V_{sat})}{0.5}$$

$$T \equiv 0.69RC.$$

3. Triggering pulse width T_p must be much smaller then T. $T_p < T$.

3. (i) Draw the schematic of ICL 8038 function generator and discuss its features(10) APR/MAY2015 , NOV/DEC2011(8)





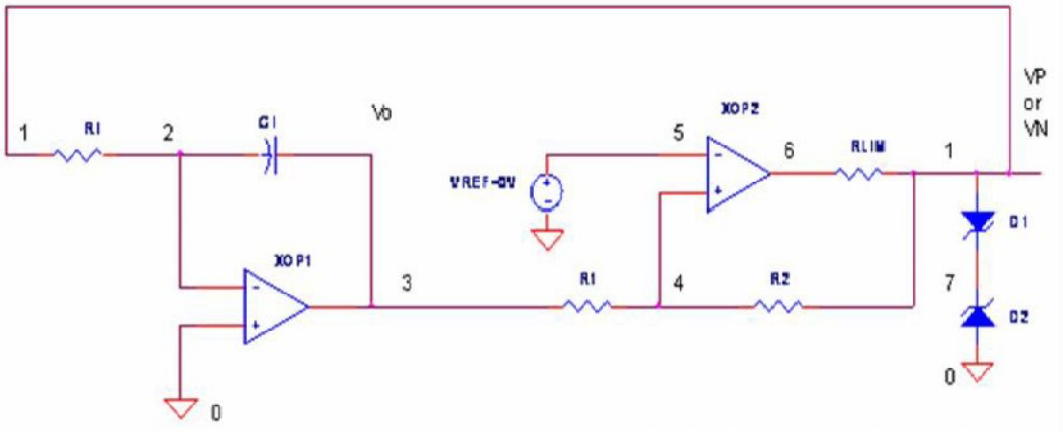
Pin 1 & Pin 12: Sine wave adjusts
Pin 2 Sine Wave Output
Pin 3 Triangular Wave output
Pin 4 & Pin 5 Duty cycle / Frequency adjust
Pin 6 + Vcc
Pin 7 : FM Bias
Pin9 : Square Wave Output
Pin 10 : Timing Capacitors
Pin 11 : -VEE or Ground
Pin 13 & Pin 14: NC

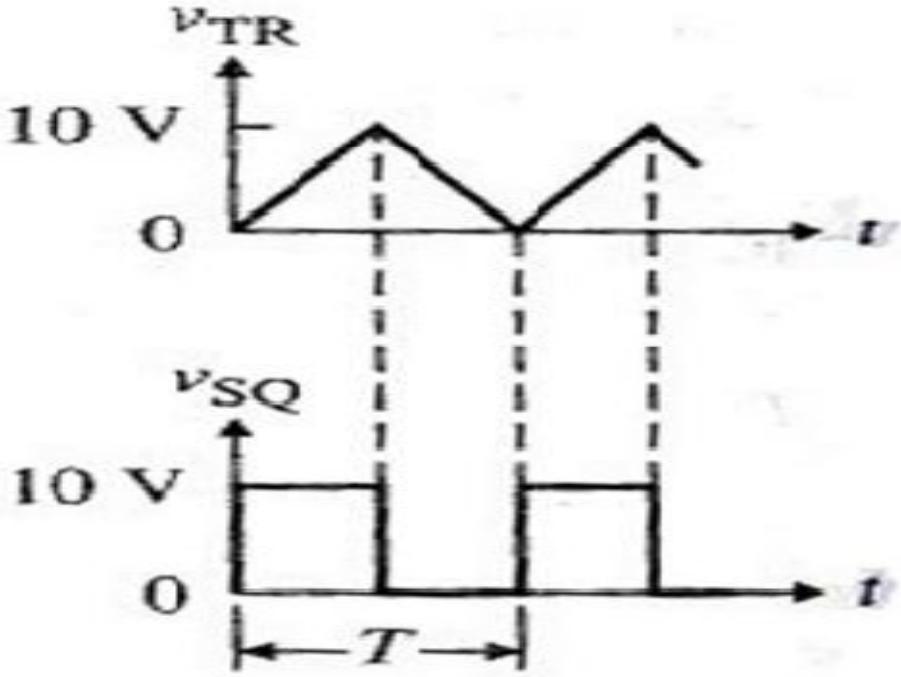
(ii) Find the expression for Frequency of Triangular waveform generator and explain the circuit (6) APR/MAY2015, APR/MAY2012 (8), APR/MAY2011 (8)

Frequency of oscillation

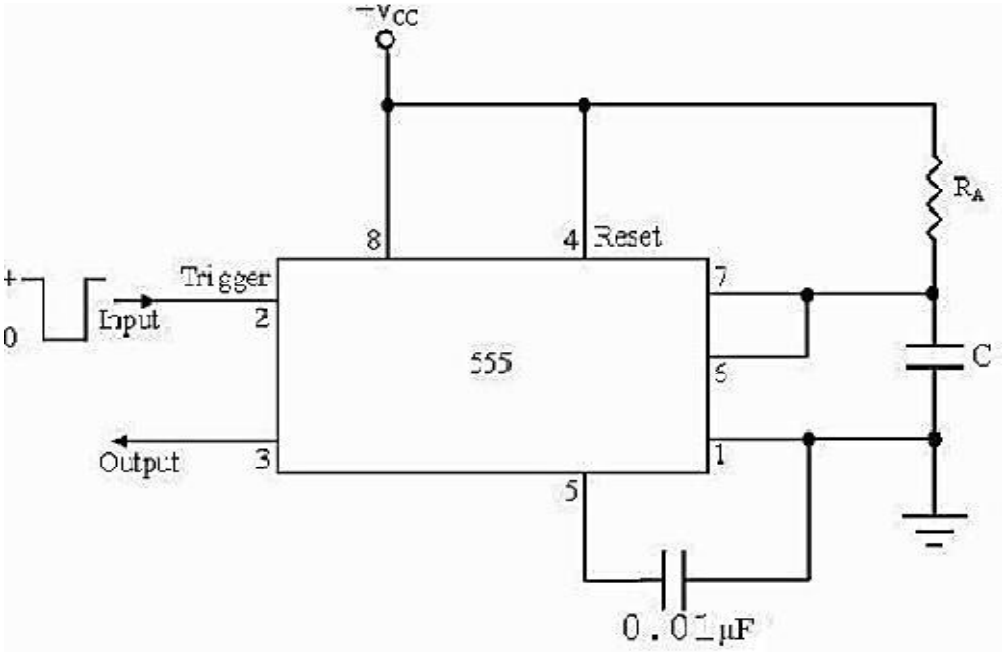
$$f_o = 1/T = R_3/4R_1C_1R_2$$

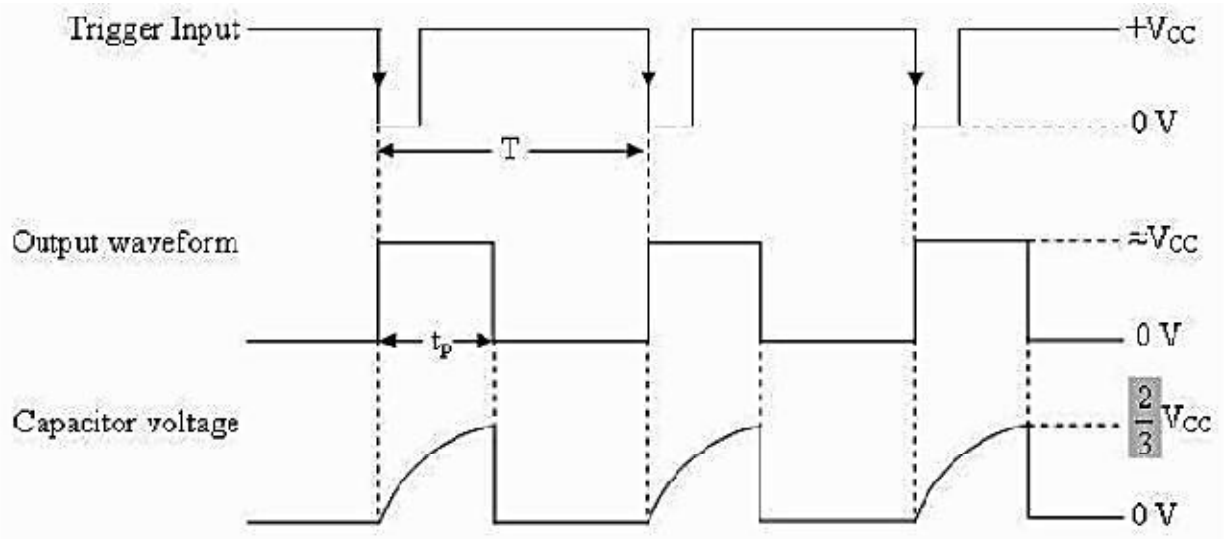
The triangle peaks and period may not accurately meet +/-10V swing at 100 us. The main reason is that current source and thresholds are derived from Zener diodes - not exactly the most accurate reference.





4. **with a neat functional diagram ,explain the working of 555 timer as monostable mutivibrator and derive an expression for the frequency of oscillation with relevant waveforms NOV/DEC 2015 (16)**





Vc = Vcc (1-e-t/RC)……. (1)
Therefore At t = T, Vc = 2/3 Vcc
2/3 Vcc = Vcc(1-e-T/RC)
or
T = RC ln (1/3)
or
T = 1.1RC seconds ……. (2)

5. **With neat circuit Diagram explain the working of linear voltage regulator using operational amplifier NOV/DEC 2015 (16),NOV/DEC2013(12)**

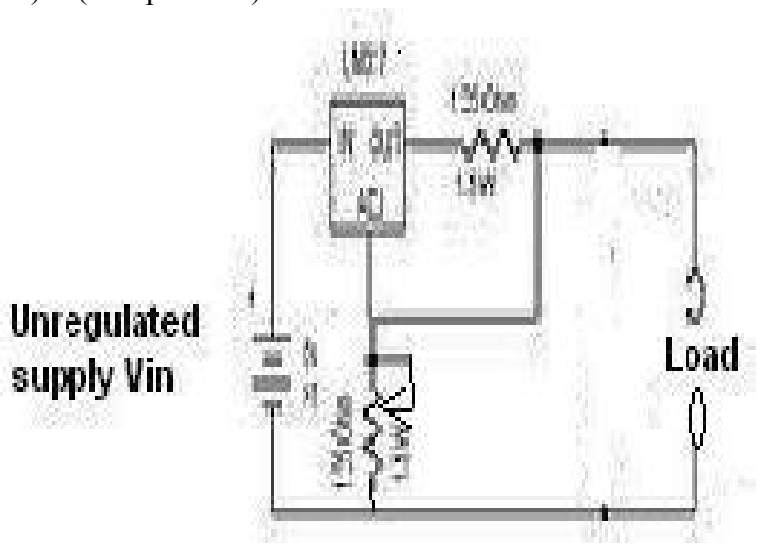
All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier. Therefore the filters are used to obtain a "steady" dc voltage from the pulsating one.

Factors affecting the output voltage:

i) IL (Load Current)

ii) VIN (Input Voltage)

iii) T (Temperature)



The output voltage

Vo is, Vo=R1I1+(I1+Iadj)R2 ---------- (1)

Where

I1= Vref/R1

Vo = (Vref/R1) R1 + Vref/R1 + Iadj R2

= Vref + (Vref/R1) R2 + Iadj R2

Vo = Vref [1 + R2/R1] + Iadj R2 ---------- (2)

R1 = Current (I1) set resistor

R2 = output (Vo) set resistor.

Vref = 1.25v which is a constant voltage between output and

Thus the final expression for the output voltage is given by

Vo= 1.25v[1 + R2/R1]

They are basically series regulators.

Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting
4. Thermal shutdown
5. Floating operation to facilitate higher voltage output

6. **Explain in detail voltage to frequency APR/MAY2014, NOV/DEC2013 and frequency to voltage converters. APR/MAY2014 (16) , APR/MAY2011(8)**

Frequency to Voltage (F-V) and voltage to frequency convertors (V-F)

F-V convertors applications:

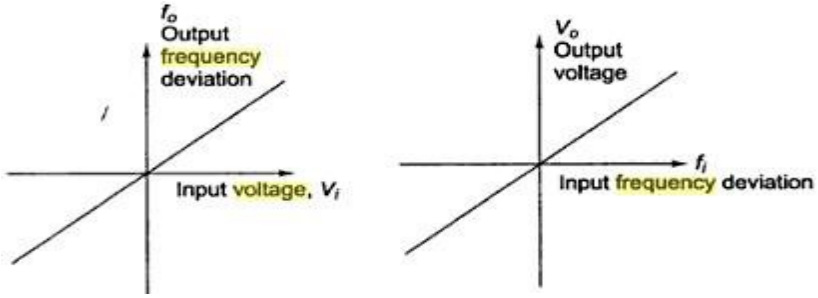
Tachometer in motor speed control

Rotational speed measurement.

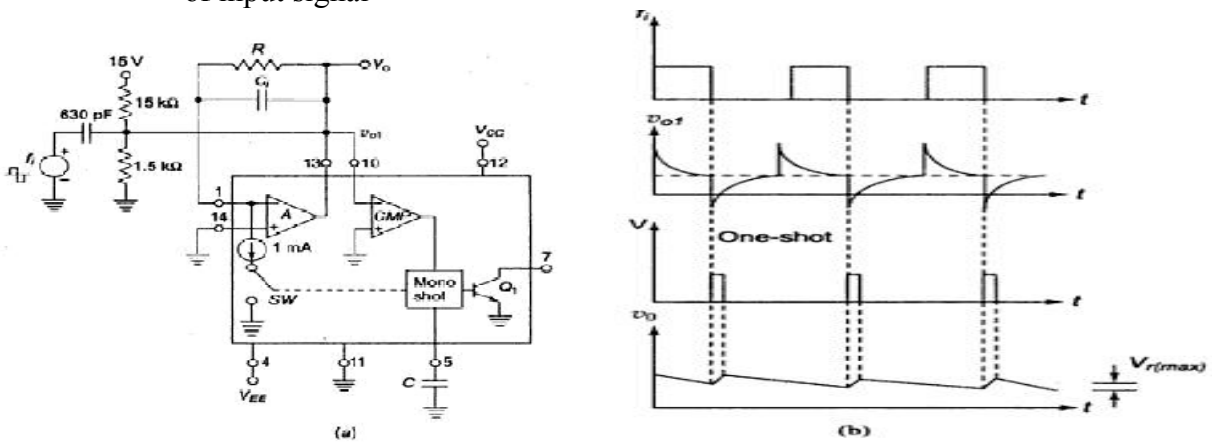
 Two types of it:

Pulse integrating

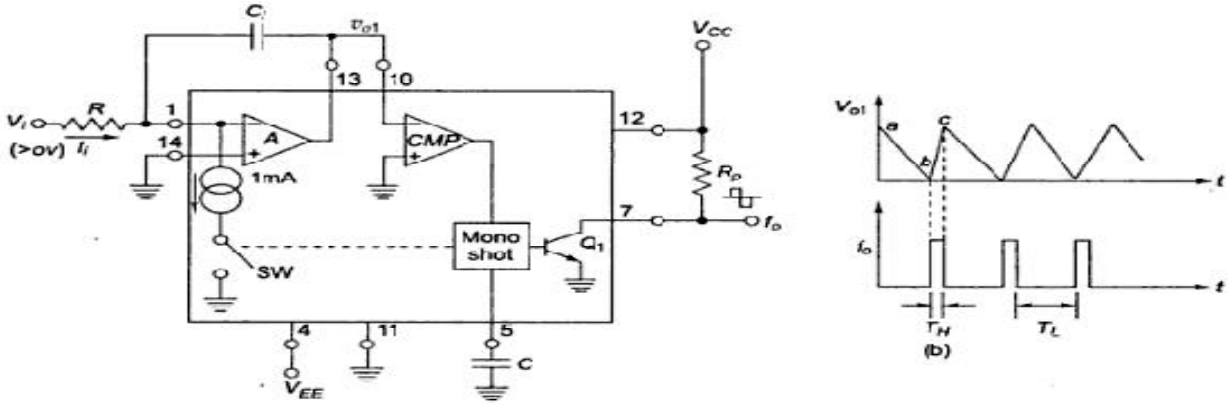
Phase locked loop



F-V convertor produces an output voltage whose amplitude is a function of input signal



Frequency To Voltage Convertor using VFC32 (V-F) and its input output characteristics



Voltage-Frequency convertor using VF32 and its input output characteristics

7. Sketch the functional block diagram of the following and explain their working principle:

(i) IC 555 Timer. (8)

(ii) General purpose voltage regulator IC 723. (8)MAY/JUNE2012

(i) IC 555 Timer NOV/DEC2011(8)

` The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

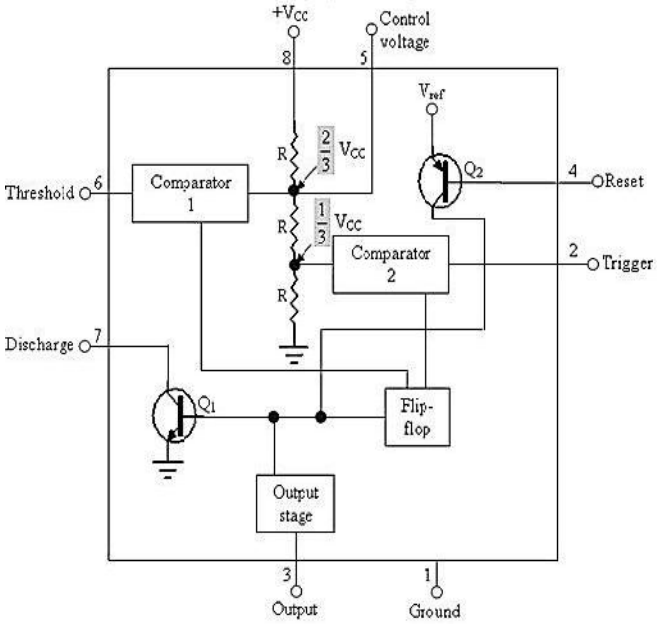
The important features of the 555 timer are these:

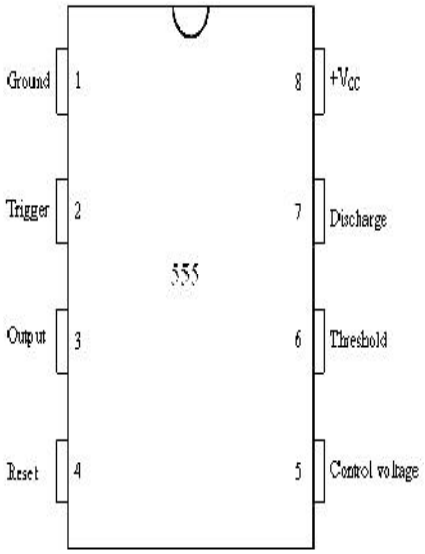
(i) It operates on +5v to +18 v supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p





Pin 1: Ground

Pin 2: Trigger

Pin 3: Output

Pin 4: Reset

Pin 5: Control voltage

Pin 6: Threshold

Pin 7: Discharge

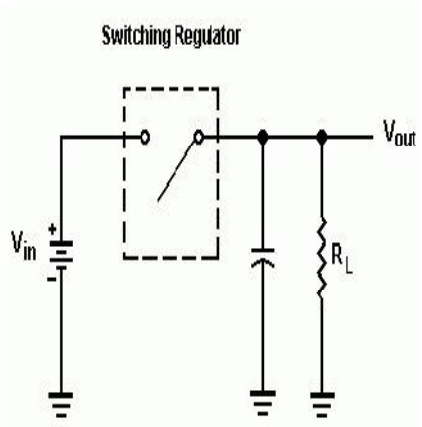
Pin 8: +Vcc

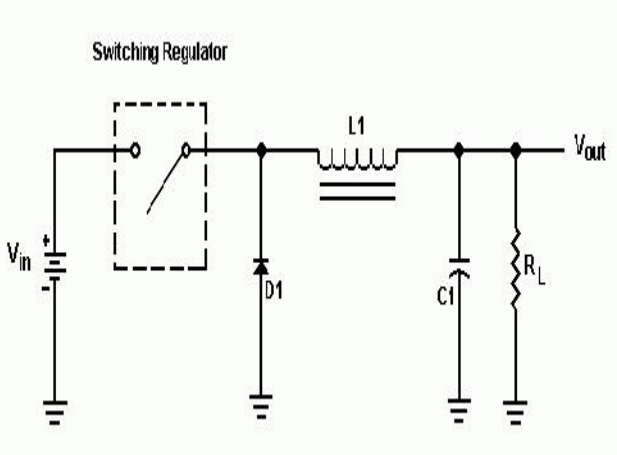
8. (i) Draw the circuit using op-amp to generate triangular wave explain its operation(8)NOV/DEC2012

(ii)with neat diagram explain the working of step down switching regulator(8) NOV/DEC2012, APR/MAY2011(8)

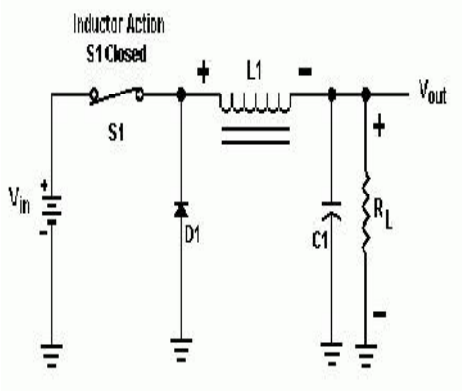
The switching regulator offers the advantages

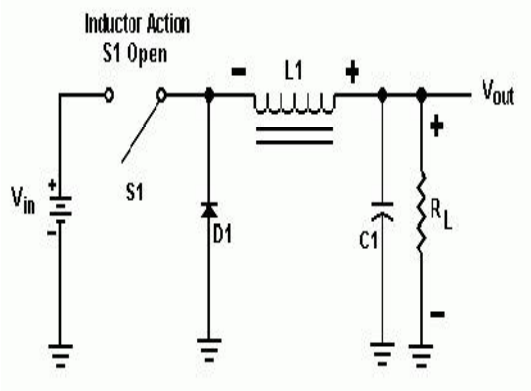
- higher power conversion efficiency
- Increased design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).
- a lot less heat and
- Smaller size.





To understand the action of D1 and L1, let's look at what happens when S1 is closed as indicated below





A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

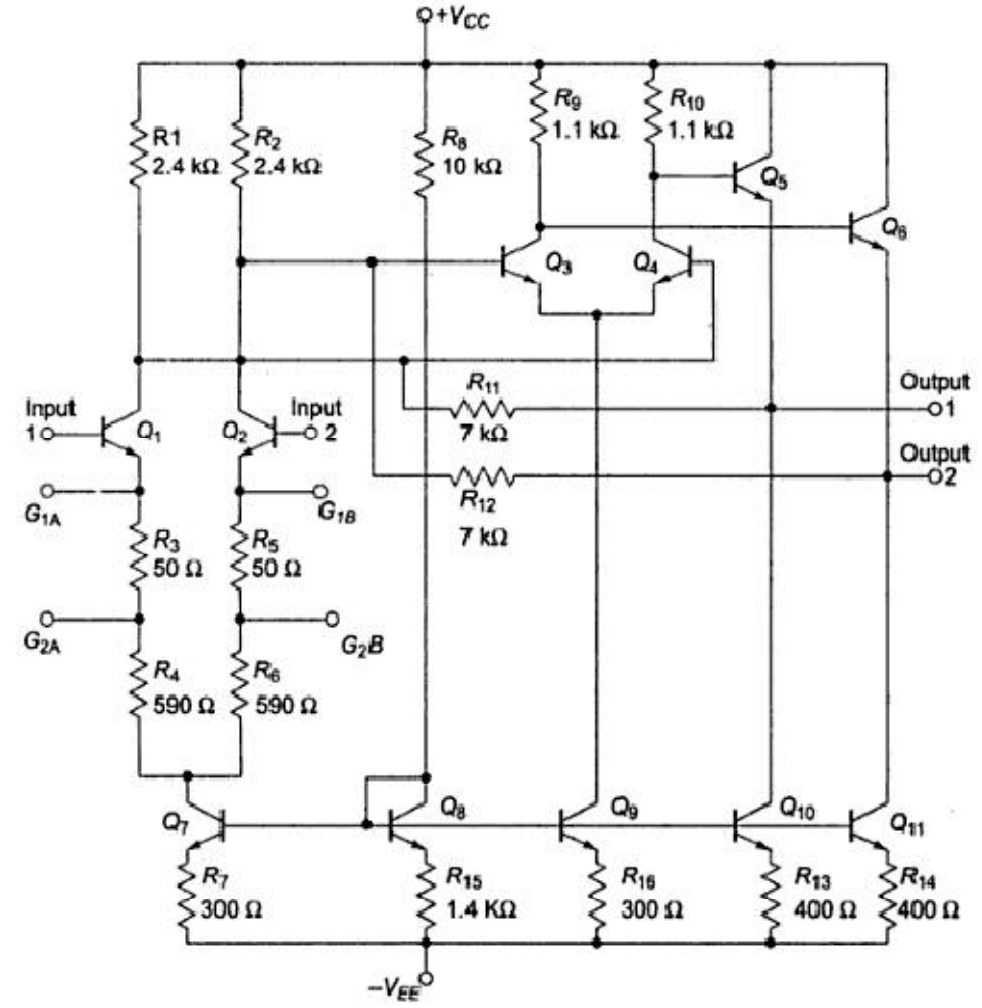
9. With suitable circuit diagram explain the working of the following

(i) video amplifier (8) NOV/DEC2012

The video or wideband amplifiers are designed to provide relatively flat gain versus frequency response characteristics for the range of frequencies required to transmit video information

Salient features:

- Wide bandwidth
- External frequency compensation not required
- Provide high common mode rejection ratio



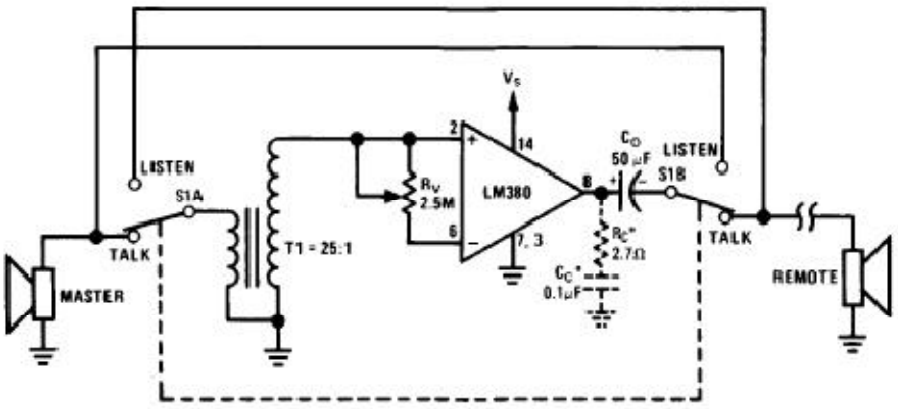
(ii) voltage to frequency converter(8) NOV/DEC2012

10. (i)with neat functional diagram explain the operation of LM380 power amplifier (8) NOV/DEC2011

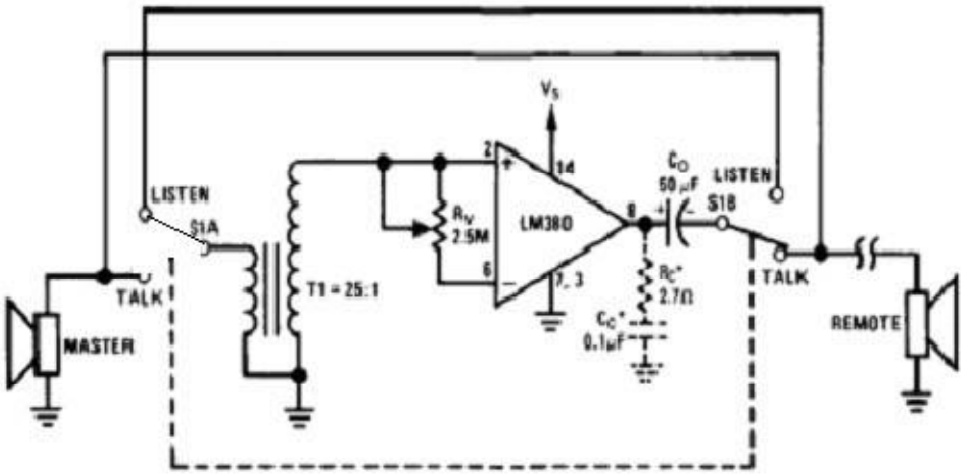
When the switch is in Talk mode position, the master speaker acts as microphone.

When the switch is in Listen position, the remote speaker acts as a microphone.

In either phone the overall gain of the circuit is the same depends on the turns of transformer T.



Talk mode



Listen mode